A 16nm 2.2pJ/b High Efficiency Pulse-Position Modulated Resonance Transceiver for 15Mbps Multi-Source High-Speed Body-Area Sensor Network

Anhang Li[1,2], Ruichen Qi[2], Yuhao Yuan[1], Juan Moya[1], Dennis Sylvester[1], and Mehdi Saligane[2]
1. EECS, University of Michigan, 1301 Beal Avenue, 48109, Ann Arbor, US
2. School of Engineering, Brown University, 184 Hope St, 02912, Providence, US
mehdi_saligane@brown.edu

***Abstract*—This paper presents a high-speed (15 Mb/s) Human Body-Coupled Communication (HBC) transceiver designed for multi-sensor applications. As the first reported HBC implementation in FinFET technology, the design achieves state-of-the-art power efficiency of 0.84 pJ/b for transmitting, with a 3.3V amplitude, and 3.2 pJ/b for receiving, by leveraging inductive resonance driving, differential-mode pulse-position modulation (DMPPM), optimized encoding density, and a power-gated receiver signal chain with peak-to-zero-crossing conversion. A multi-sensor transaction demo is presented.**

Keywords—human body channel, data transceiver, low power, FinFET

I. Introduction

Recently, Human Body-Coupled Communication (HBC) techniques, such as Electrical-Quasistatic HBC and Galvanically Coupled HBC, have become attractive options for building a body-wide sensor network (Fig. 1) due to their ultra-high power efficiency compared to alternatives, including BLE and Wi-Fi. The E-field of the human body channel in the 10kHz~30MHz range wraps around the body and does not leak into the air [2], making it also attractive for data confidentiality considerations.

The HBC channel is primarily capacitive, resulting in a high αCV^2f switching loss with a simple CMOS driver. Prior work explored on-chip switched capacitor circuits [1] to drive such loads. These circuits improve energy efficiency. However, the capacitance of the switched-capacitor circuit depends on the electrode and skin properties and does not scale with CMOS technology. In FinFET, a high-Q 80 pF capacitor occupies a substantial area that would otherwise be used for digital circuits.

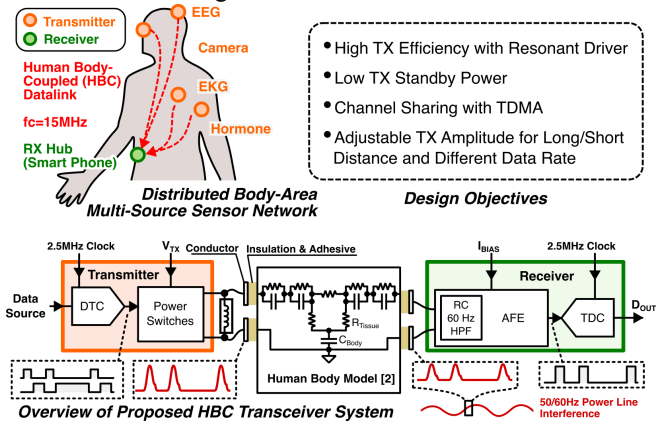

Figure 1. Overview of the Design Objectives, and Proposed HBC Transceiver System Implementation

We present a 16 nm FinFET HBC datalink with a series-resonant inductive transmitter operating at 15 Mbps carrier frequency. Prior art [6] has explored OOK modulation with a resonant driver; however, the reported power efficiency and speed are underwhelming due to the tradeoff between bandwidth and resistive loss in RLC resonators. We combine a high-Q resonant TX with a differential-mode single-pulse pulse-position modulation (DMPPM) scheme [3]. This improves TX power efficiency by 80% (from 4.2pJ/b to 0.85pJ/b) and enables a 2x VDD swing without transistor stress, reaching a maximum amplitude of 3.3V with 16nm FinFET.

Combined with a DMPPM receiver (RX) featuring an open-loop design and dynamic power control, the TX-RX pair can achieve a 50% power efficiency improvement with one TX and one RX; adding more TXs will further enhance efficiency. Due to the demonstrated energy efficiency advantage, we propose constructing a multiple-transmitter sensor network (Fig. 1) that can be deployed on the human body or a surface with similar characteristics.

II. Energy-Efficient Resonant Transmitter

	Abstracted Circuit	Pulse Profile & Ideal SW Power	Pros & Cons
CMOS Driver	C_{LOAD}	CMOS Rise & Fall $P=CV^2f_{REP}/2$	✗ Low energy efficiency ✓ Simple control ✗ High-frequency content ✓ Small on-chip area
Switched Capacitor [1]	C_{LOAD}	$N_{STAIRS}=4$ Multi-Level CMOS Rise & Fall $P=CV^2f_{REP}/2N_{STAIRS}$	✓ High energy efficiency ✗ Complex control ✗ High-frequency content ✗ Large on-chip capacitor (80pF)
Inductive Resonance	**This Work** Pass C_{LOAD}	Sinusoidal Rise & Fall $P=\pi RV^2f_{REP}C^{3/2}/4L^{1/2}$ (RLC Resonator)	✓ High energy efficiency ✓ Simple control ✓ Bandwidth control w/o LPF ✓ Small on-chip area ✗ Requires off-chip inductor

*f_{REP} is the pulse repetition rate

Figure 2. Comparison of HBC Transmitter Designs

To drive the capacitive load efficiently, we propose an energy recovery circuit using a single off-chip inductor to resonate with the load. In ideal conditions, this approach offers power consumption that is orders of magnitude lower than similar techniques, leveraging the much higher Q of off-chip inductors (>40) compared to on-chip passives(Fig. 2). Another advantage of this inductor driving scheme is that the pulses are perfect sinusoids, which avoids out-of-band high-frequency content and allows for the elimination of off-chip EMC filtering passive components required by prior work. The

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proposed technique effectively limits high-frequency harmonics (Fig. 3) in the band that can leave the skin and radiate into the air (>30MHz [2]), thereby reducing the associated information confidentiality risks. It should be noted that an off-chip discrete inductor may limit form-factor scaling; therefore, the choice of technique should be application-dependent.

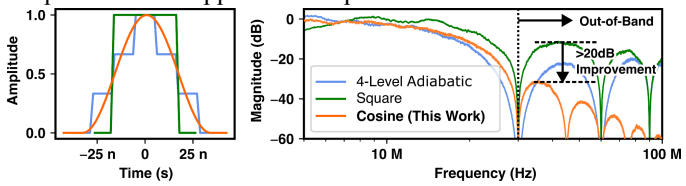

Figure 3. Simulated Spectrum Comparison of TX Pulseshapes (Normalized to the same amplitude and bandwidth)

The circuit implementation (Fig. 4, 5) relies on a single pass-gate MOSFET driven by a simple 1ns-resolution delay-line TDC to initiate sinusoidal LC resonance from a steady state. Once the resonance has completed one full sine wave cycle, the passgate is closed, and a small reset MOSFET is activated to remove any residual voltage caused by parasitic losses. The output amplitude is 2x the input voltage VTX. At maximum, the chip can produce a 3.3V pulse at the output node with VTX = 1.7V. Unlike the passgate, which needs to fully switch on in <1 ns to minimize conduction loss, the reset switch only needs to discharge the residual voltage over a large time window (> 200 ns); a small transistor with cascode shielding is sufficient, adding negligibly to the output capacitance. The chip also features a small 16pF on-chip tunable capacitor to trim any frequency mismatch, thereby achieving optimal efficiency. This on-chip capacitor has significantly lower Q (<10) than the actual load capacitance due to resistive parasitics, so it should be kept small. The effectiveness of this foreground calibration technique is discussed in Section V.

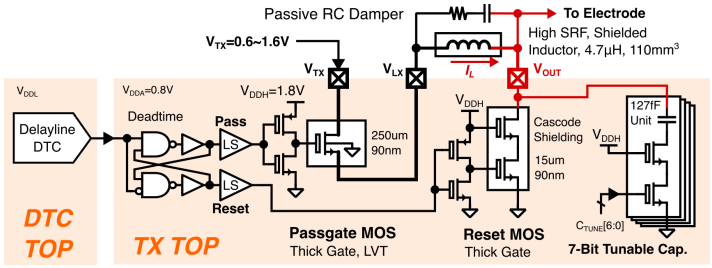

Figure 4. Proposed Resonant TX Circuit

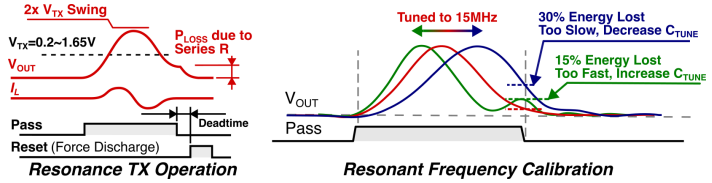

Figure 5. TX Operation, and Capacitance Calibration Process

III. Energy-Efficient Amplitude-Insensitive DMPPM Receiver

Fig. 6 shows the receiver, which is based on a chain of open-loop amplifiers and enables optimal power efficiency performance under the low voltage headroom limitation of FinFET transistors. Monte Carlo simulations show that the 3σ input-referred offset is <1.0 mV. The received pulse suffers from a random amplitude variation due to mechanical movement and LC parasitics. These are not problematic for low encoding density applications, but lead to issues at the 6-bit per pulse high-speed mode because the rising edge at a 15 MHz carrier frequency is approximately 30 ns, and the amplitude change, combined with a fixed threshold, causes more than 4 ns of timing error regardless of thermal noise. To overcome this limitation, we implemented an HPF-based differentiation circuit that converts the peak of the incoming unipolar pulse to a zero-crossing bipolar pulse[4]. The waveforms measured at the output of the HPF (Fig. 7) show that when tuned to the same frequency as the TX circuit, the received peak position is no longer amplitude-dependent and can be easily digitized; this is achieved by trading off a 3 dB SNR.

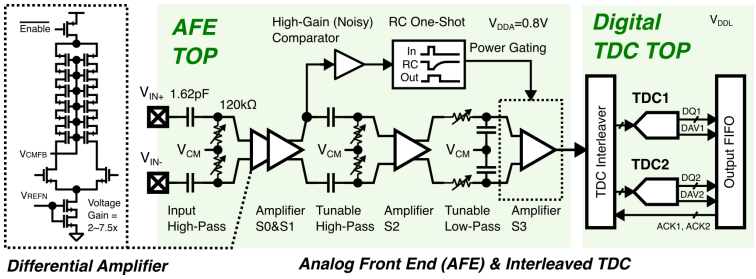

Figure 6. Receiver Implementation

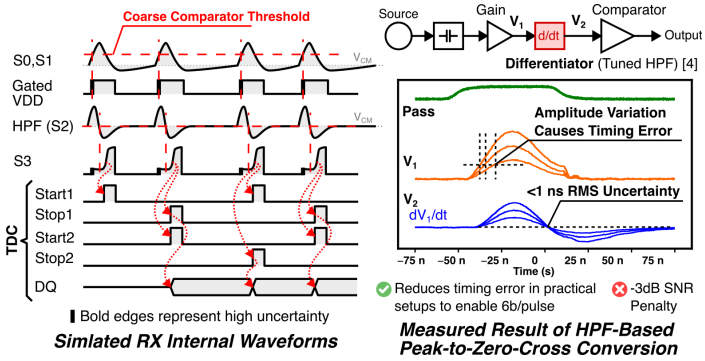

Figure 7. Timing Diagram and Measured Result of the HPF-based Differentiator

The final step of AFE amplification is to convert the zero-crossing point into a square wave with sharp and accurate rising edges, a challenging task that demands high speed, high gain, and thus high power consumption. To overcome this challenge, we add a coarse pulse detector path that conservatively detects the presence of a pulse. The threshold of the coarse detector is lower than that of the fine detector by 50mV. The threshold gap is chosen to be sufficiently large such that the background noise of the application environment causes fewer than BER = 1E-3 false positives. Upon firing, the coarse detector releases power gating of the fine detector, which enters its operating state in less than 20 ns to capture the zero-crossing in time. An RC one-shot circuit with a time constant of 100ns controls the power-on duration of the fine detector and prevents rapid toggling in the presence of noise. This modification enables the use of a 20uW high-power continuous-time comparator in the final stage, resulting in a 29% power reduction (from 63.5uW to 45.4uW). Following the AFE, a time-interleaved coarse-fine ring-oscillator-based TDC circuit [5] operating at 0.4V digitizes the amplified edges and pushes them to a digital FIFO.

IV. DMPPM Modulation

Inspired by recent advances in ultra-wideband (UWB) radios, we implemented DMPPM modulation in which the time interval between two pulses represents a 1~6-bit data symbol [3]. Compared to prior art [1] using combinational pulse position modulation (CPPM), DMPPM has 70% less switching activity along with more time between pulses, enabling lower inter-symbol-interference (ISI). However, the design relies on high-accuracy DTC and TDC circuits to produce and measure the sub-clock pulse timing.

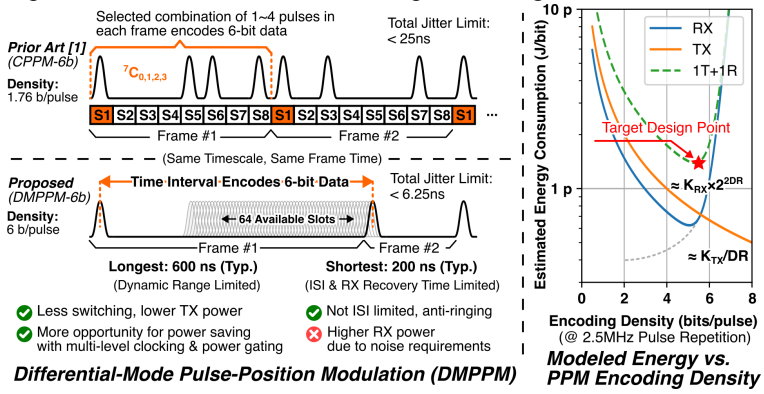

Figure 8. DMPPM Modulation and Design Point Optimization

The optimal encoding density (i.e., bits-per-pulse, BPP) is determined with the following model-based analysis:

- The TX only needs to transmit a single pulse per frame, and the DTC power is negligible compared to the power dissipated by the transistors. Increasing BPP improves energy efficiency.
- At lower encoding density, RX power primarily comes from static power and leakage. Increasing BPP improves energy efficiency.
- At high encoding density, RX power primarily comes from timing noise requirements. Increasing BPP exponentially decreases energy efficiency.

Based on simulation data, we can create an energy vs. encoding density plot (Fig. 8), which shows that the optimal BPP number is approximately 6.

V. Experimental Results

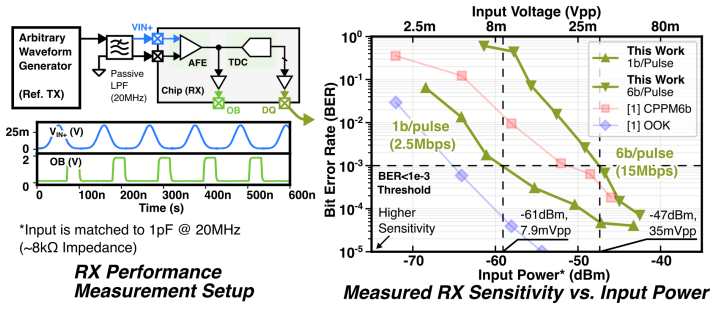

Figure 9. Measured BER Plot

Fig. 9 shows the BER performance of our TX-RX pair at the optimal efficiency point. Due to the higher encoding density of DMPPM, the RX sensitivity is inferior to that of the prior art [1] (-47 dBm vs. -52 dBm). However, the resonant TX allows us to compensate for it with higher TX power (3.3Vpp vs. 0.7Vpp driving the same impedance) without significantly increasing the system power consumption.

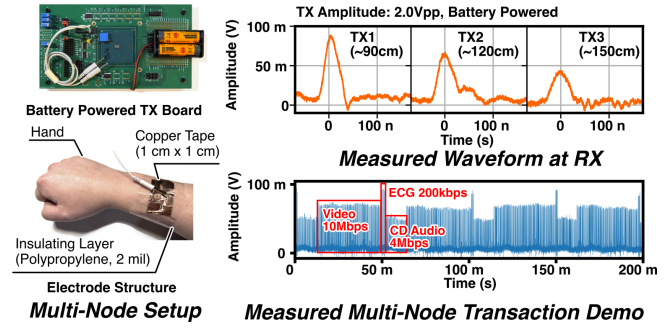

Figure 10. Measured Time-Domain Waveforms at the Receiver and Multi-Node Transaction Demonstration

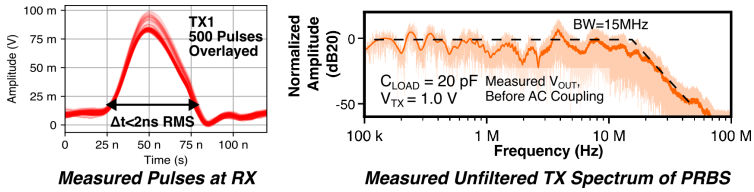

Figure 11. Visualization of Jitter, and TX Spectrum

A multi-node setup is presented (Fig. 10), featuring battery-powered transmitters placed at various locations on the body. The capacitively coupled electrode is composed of a 2-mil layer of polypropylene tape and a 1 cm² copper tape conductor. The demo showcases a 10 Mbps video stream, a 4 Mbps audio stream, and a 200 kbps 12-lead digitized ECG data stream transmitted simultaneously over the human body channel using time division multiple access (TDMA). Based on the experiment results, with a 2Vpp transmitting amplitude, the presented HBC transceiver can transmit and receive with BER<1E-3 at any location on the body with no noticeable short-term frequency shift (Fig. 11). The bandwidth is also limited, as predicted by the simulation. In particular, the TX2 waveform exemplifies a multi-path effect, characterized by a second peak that appears after the main pulse. Our design is resilient to this kind of interference.

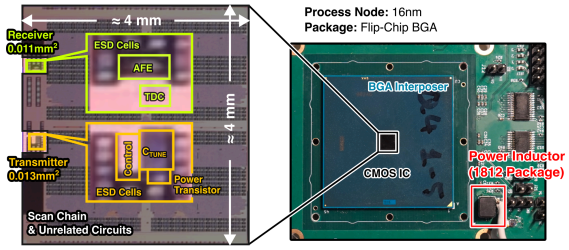

Figure 12. Chip Micrograph & Assembly

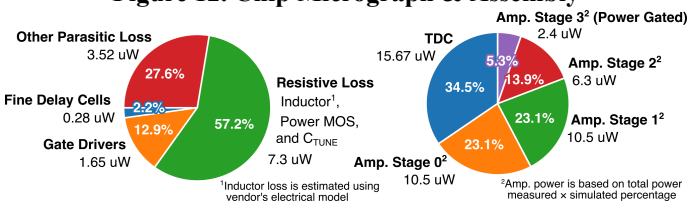

Figure 13. Measured Power Consumption Breakdown

Fig. 12 shows the chip photograph, packaging, and PCB layout photographs. The high self-resonant-frequency (SRF) inductor, with shielded 1812 packaging, is placed in proximity to the chip and electrode to minimize resistive loss. Fig. 13 shows a detailed power breakdown of the TX-RX pair when operating at its highest power efficiency point.

VI. Conclusion

Table 1 and Fig. 14 compare the test-chip performance with that of state-of-the-art wearable HBC transceivers [1,6,7,8,9,10]. The presented design is the first HBC transceiver implemented in FinFET technology. It achieves the highest system power efficiency among recently reported HBC transceivers, with balanced power and data rates [1,6,7,8,9,10,11,12,13,14]. In particular, the bar plot shows that our TX circuit, with a leakage power of approximately 280 nW, also exhibits the lowest power consumption compared to circuit designs optimized for low absolute power & low data rate applications [6,7,10], making it attractive for ECG, EEG, and other monitoring applications where the transmitting sensor node is duty-cycled and can stay in hibernation most of the time.

Paper	This Work	B.Chatterjee, ISSCC'22 [1]	N. Modak CICC'21 [6, 10]	S.Maity JSSC'21 [7]	J. Park, ISSCC'19 [8]	S.Maity JSSC'19 [9]
Technique	Inductor Resonance	Adiabatic Switching	Inductor Resonance	CMOS Push-Pull	Push-Pull, Magnetically Coupled	CMOS Push-Pull
Modulation	DMPPM6b	CPPM (3~6b)	OOK	OOK	OOK	NRZ
Demod. Method	TDC + DTC	CDR	CDR	CDR	Env. Detect	CDR
Carrier Freq.	15 MHz	20 MHz	0.5~2 MHz	0.05~1 MHz	40 MHz	-
Data Rate (Mbps)	2.5~15	7.5~15	0.001~0.02	0.001~0.02	5	30
VDD (V)	0.8	0.75	0.5	0.5	0.6	1
Maximum TX Amplitude w/o Stress (V)	3.3	0.7	10	0.5	-	-
Best TX Energy (pJ/b)	0.85, 2Vpp (6 b/p)	4.2, 0.7Vpp (NRZ CPPM-6b)	169	277.9	11.2	34.9
Best RX Energy (pJ/b)	3.2 (6 b/p)	4.0 (NRZ CPPM-6b)	3.6	140	4.8	3.27 (w/o Clock)
TX Power (uW)	12.75	63	1.5	2.47	35.8	2600
RX Power (uW)	48	60	72	1.4	24	98
Area (mm^2)	RX: 0.011 TX: 0.013	0.259	0.13	0.3375	0.12	
Process Node	16nm	65nm	65nm	65nm	65nm	65nm
Sensitivity (dBm)	-47 (6 b/p) -61 (1 b/p)	-65 (OOK) -52 (CPPM)	-60	-64	-56	-64
BER Target	1E-3	1E-3	1E-5	1E-3	1E-3	1E-3

Table 1. Comparison Table of SoTA HBC Transceivers

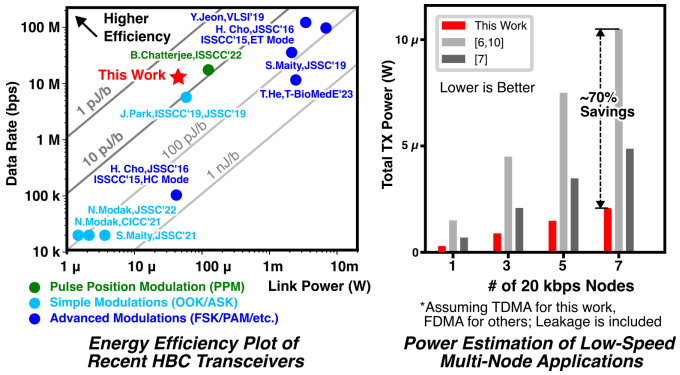

Figure 14. Comparison Chart of SoTA HBC Transceivers, and Comparison of Low Data Rate TX Applications

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References

[1] B. Chatterjee, A. Datta, M. Nath, G. K. K, N. Modak, and S. Sen, "A 65nm 63.3µW 15Mbps Transceiver with Switched-Capacitor Adiabatic Signaling and Combinatorial-Pulse-Position Modulation for Body-Worn Video-Sensing AR Nodes," 2022 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2022, pp. 276-278.

[2] S. Maity, M. He, M. Nath, D. Das, B. Chatterjee, and S. Sen, "Bio-Physical Modeling, Characterization, and Optimization of Electro-Quasistatic Human Body Communication," in IEEE Transactions on Biomedical Engineering, vol. 66, no. 6, pp. 1791-1802, June 2019.

[3] G. Lee, J. Jang, J. -H. Kim and T. W. Kim, "An IR-UWB CMOS Transceiver With Extended Pulse Position Modulation," in IEEE Journal of Solid-State Circuits, vol. 57, no. 8, pp. 2281-2291, Aug. 2022.

[4] K. Li, S. Su, Z. Huang, Y. Zhao, and J. Guo, "A Low Walk Error Timing Discrimination ASIC With Rail-to-Rail Dynamic Range and ICMR for Pulsed ToF LiDAR Receiver," in IEEE Transactions on Instrumentation and Measurement, vol. 74, pp. 1-13, 2025, Art no. 2005713.

[5] M. Z. Straayer and M. H. Perrott, "A Multi-Path Gated Ring Oscillator TDC With First-Order Noise Shaping," in IEEE Journal of Solid-State Circuits, vol. 44, no. 4, pp. 1089-1098, April 2009, doi: 10.1109/JSSC.2009.2014709.

[6] N. Modak et al., "A 65nm Resonant Electro-Quasistatic 5-240uW Human Whole-Body Powering and 2.19uW Communication SoC with Automatic Maximum Resonant Power Tracking," 2021 IEEE Custom Integrated Circuits Conference (CICC), Austin, TX, USA, 2021, pp. 1-2.

[7] S. Maity et al., "Sub-µWRComm: 415-nW 1–10-kb/s Physically and Mathematically Secure Electro-Quasi-Static HBC Node for Authentication and Medical Applications," in IEEE Journal of Solid-State Circuits, vol. 56, no. 3, pp. 788-802, March 2021.

[8] J. Park and P. P. Mercier, "17.6 A Sub-40µW 5Mb/s Magnetic Human Body Communication Transceiver Demonstrating Trans-Body Delivery of High-Fidelity Audio to a Wearable In-Ear Headphone," 2019 IEEE International Solid-State Circuits Conference - (ISSCC), San Francisco, CA, USA, 2019.

[9] S. Maity, B. Chatterjee, G. Chang, and S. Sen, "BodyWire: A 6.3-pJ/b 30-Mb/s −30-dB SIR-Tolerant Broadband Interference-Robust Human Body Communication Transceiver Using Time Domain Interference Rejection," in IEEE Journal of Solid-State Circuits, vol. 54, no. 10, pp. 2892-2906, Oct. 2019.

[10] N. Modak et al., "EQS Res-HBC: A 65-nm Electro-Quasistatic Resonant 5–240 µW Human Whole-Body Powering and 2.19 µW Communication SoC With Automatic Maximum Resonant Power Tracking," in IEEE Journal of Solid-State Circuits, vol. 57, no. 3, pp. 831-844, March 2022.

[11] H. Cho et al., "A 79 pJ/b 80 Mb/s Full-Duplex Transceiver and a 42.5µW 100 kb/s Super-Regenerative Transceiver for Body Channel Communication," in IEEE Journal of Solid-State Circuits, vol. 51, no. 1, pp. 310-317, Jan. 2016.

[12] H. Cho, H. Kim, M. Kim, J. Jang, J. Bae, and H.-J. Yoo, "21.1 A 79pJ/b 80Mb/s full-duplex transceiver and a 42.5µW 100kb/s super-regenerative transceiver for body channel communication," 2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers, San Francisco, CA, USA, 2015, pp. 1-3.

[13] T. He et al., "A Re-Configurable Body Channel Transceiver Towards Wearable and Flexible Biomedical Sensor Networks," in IEEE Transactions on Biomedical Circuits and Systems, vol. 17, no. 5, pp. 1022-1034, Oct. 2023.

[14] Y. Jeon et al., "A 100Mb/s Galvanically-Coupled Body-Channel-Communication Transceiver with 4.75pJ/b TX and 26.8 pJ/b RX for Bionic Arms," 2019 Symposium on VLSI Circuits, Kyoto, Japan, 2019, pp. C292-C293.