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IEEE Custom Integrated Circuits Conference

14.8: A 16nm 2.2pJ/b High Efficiency Pulse-Position Modulated Resonance Transceiver for 15Mbps Multi-Source High-Speed Body-Area Sensor Network

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Outline

- Motivation
- The Proposed Sensor Node TRX Design
    - High Density Differential-Mode Pulse-Position-Modulation (DM-PPM)
    - Resonant Pulse Transmitter
    - Low Power Receiver
- Measurements & Conclusion

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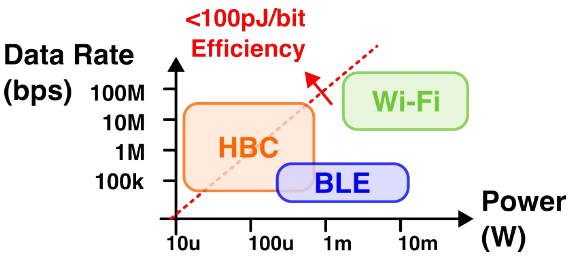
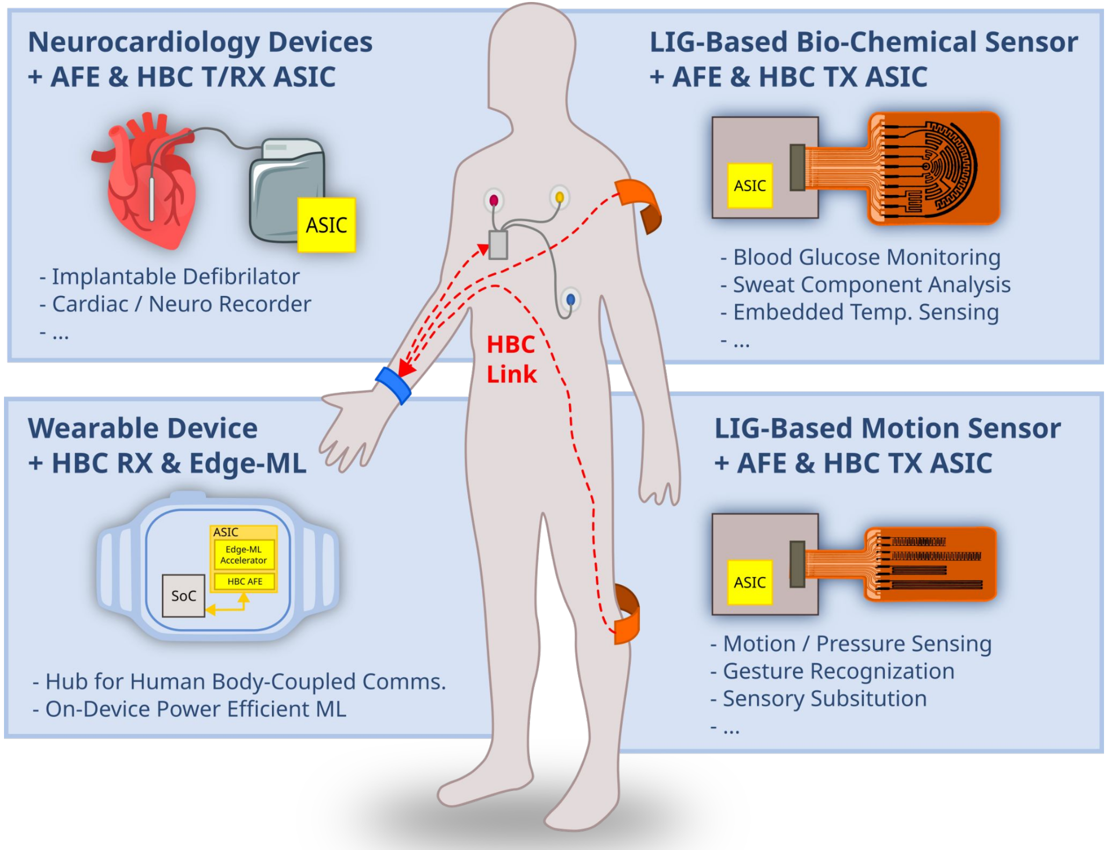
Motivation

Communication of Sensor nodes

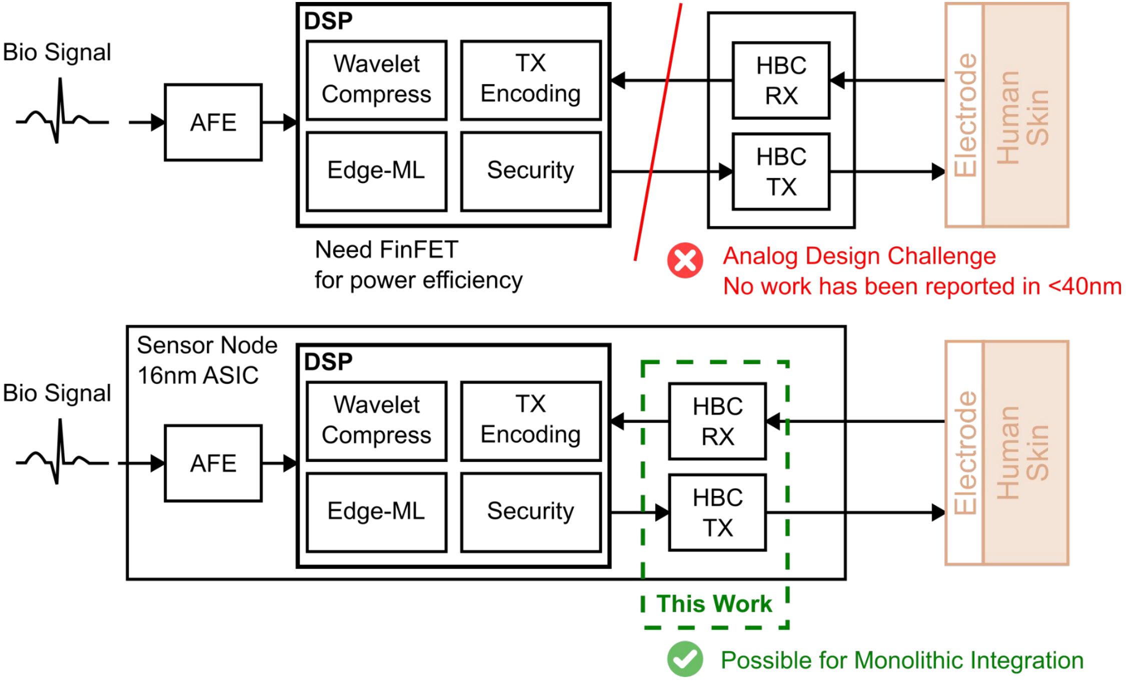
- Monitoring
- Bio Signature
- Neuro-Implant
- …

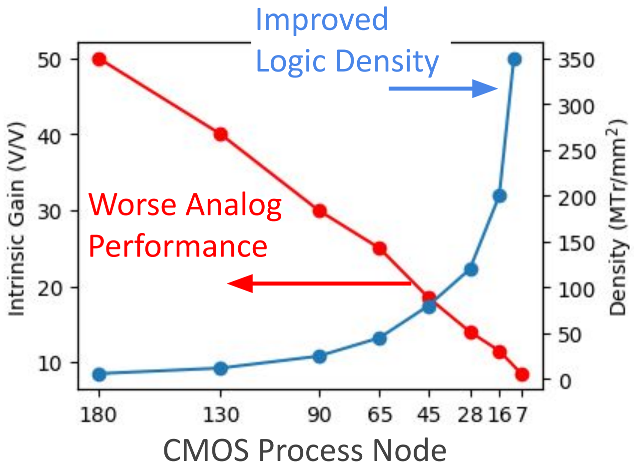
HBC provides much higher energy efficiency than 2.4GHz radio.





Challenge: Integrating HBC AFE with Digital Processor





Challenge: Advanced nodes have high leakage and low headroom

No reported HBC transmitter in FinFET nodes

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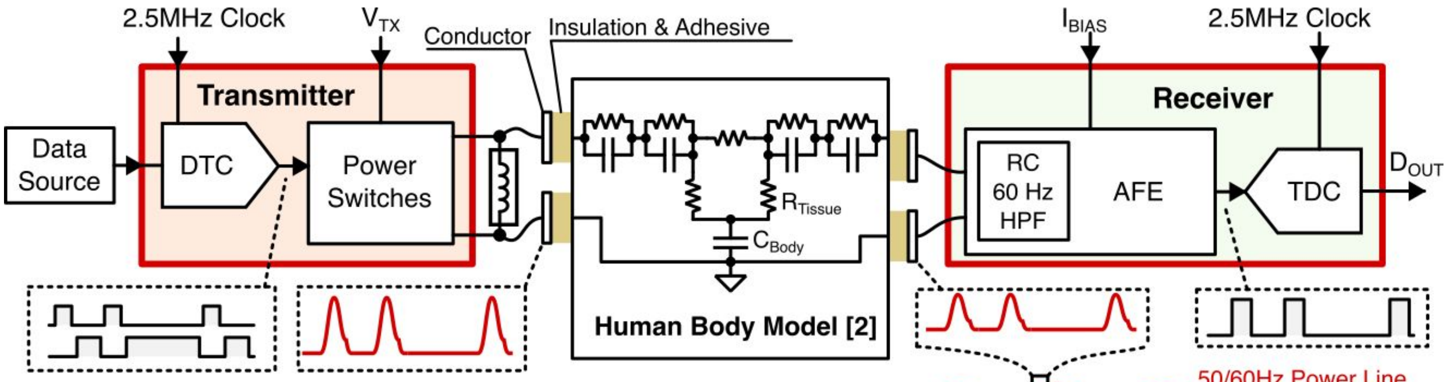
Overview of the Proposed TRX System



Overview of Proposed HBC Transceiver System

- Reduce pulse-per-bit → Better encoding scheme (DM-PPM)
- High efficiency TX → Use of High-Q Inductor
- High efficiency RX → FinFET-Optimized Circuit; Power Management Techniques

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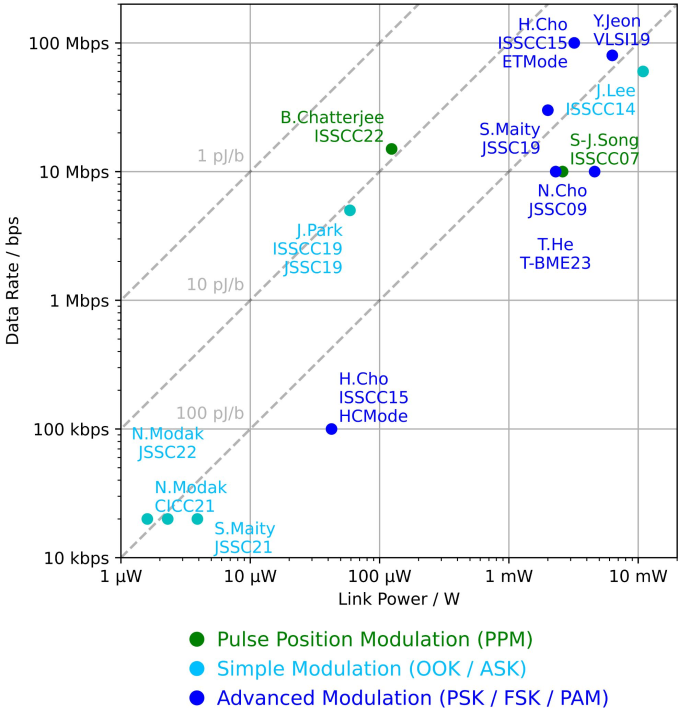
Modulation Schemes in Prior Arts



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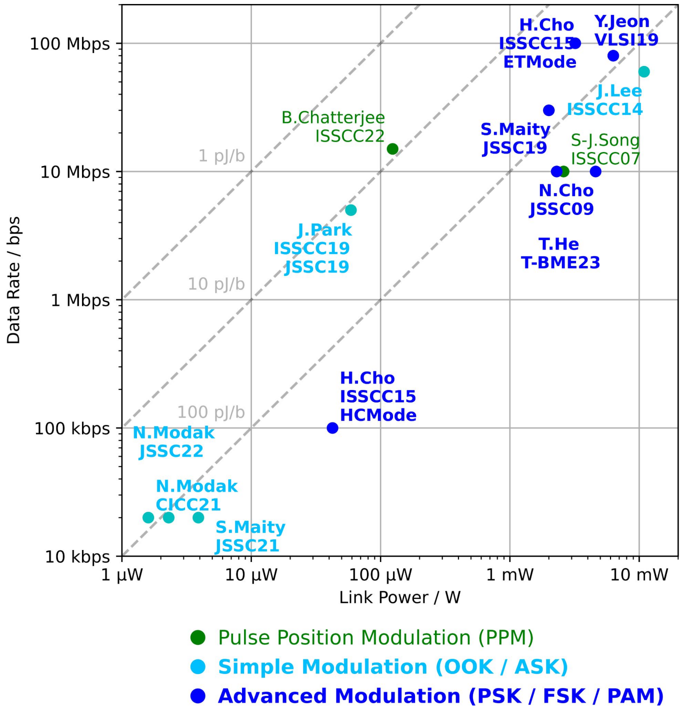
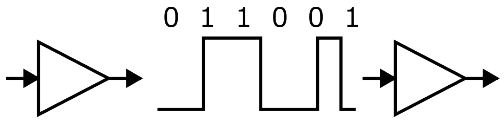
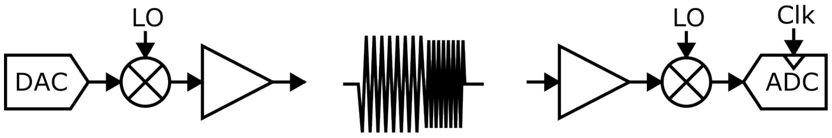




RZ/NRZ Signal

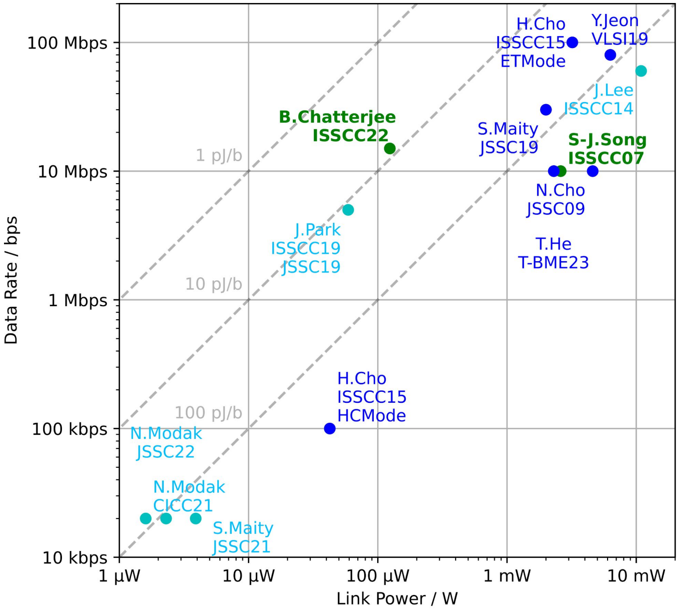
- ✔ Simple
- ✖ Low Data Rate
- ✖ Susceptible to Interference



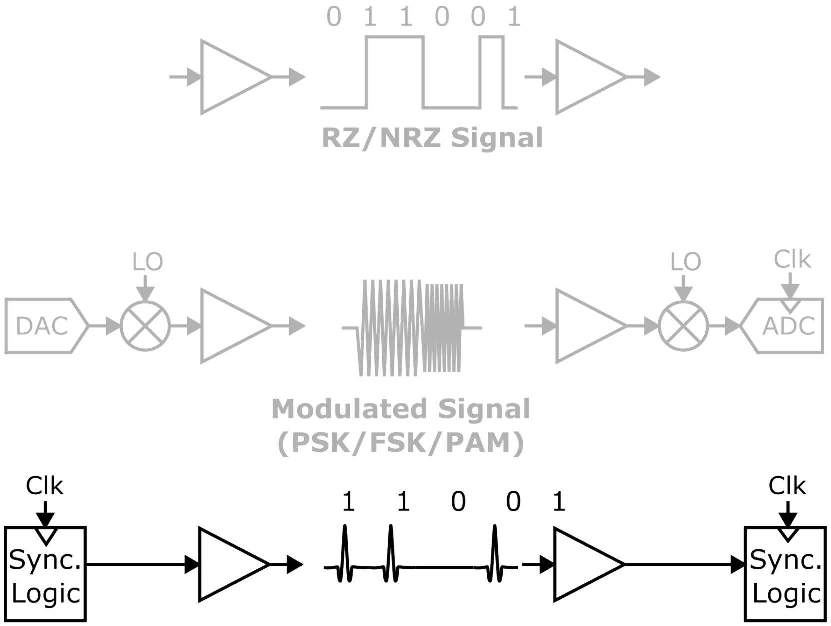
Modulated Signal (PSK/FSK/PAM)

- ✔ High Data Rate (>50Mbps)
- ✔ Good Efficiency for High Data Rate
- ✖ High Power for Mid/Low Data Rate
- ✖ High Design & Calibration Complexity

Modulation Schemes in Prior Arts



- **Pulse Position Modulation (PPM)**
- Simple Modulation (OOK / ASK)
- Advanced Modulation (PSK / FSK / PAM)

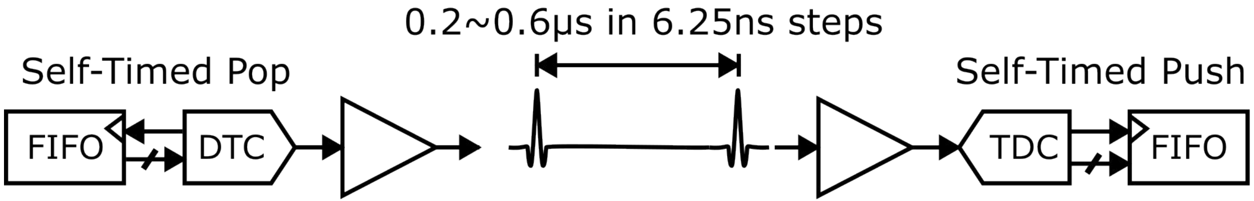


Pulse Position Modulation

- High Data Rate (~15Mbps)
- Low Power with Less Switching Activity
- Simple to Design & Calibrate
- Clock Rate limits Data Rate

High Density Differential-Mode Pulse-Position-Modulation (DM-PPM)

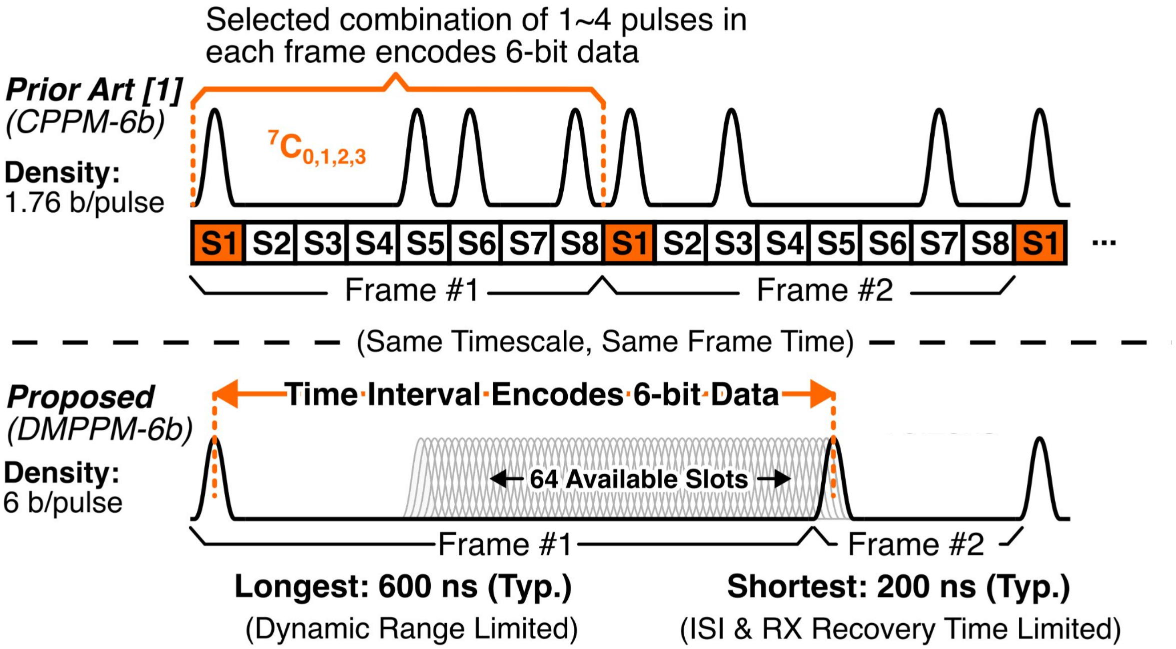
Proposed Fully Asynchronous Time-Domain Signaling



Modulated Signal (Pulse-Position Modulation)

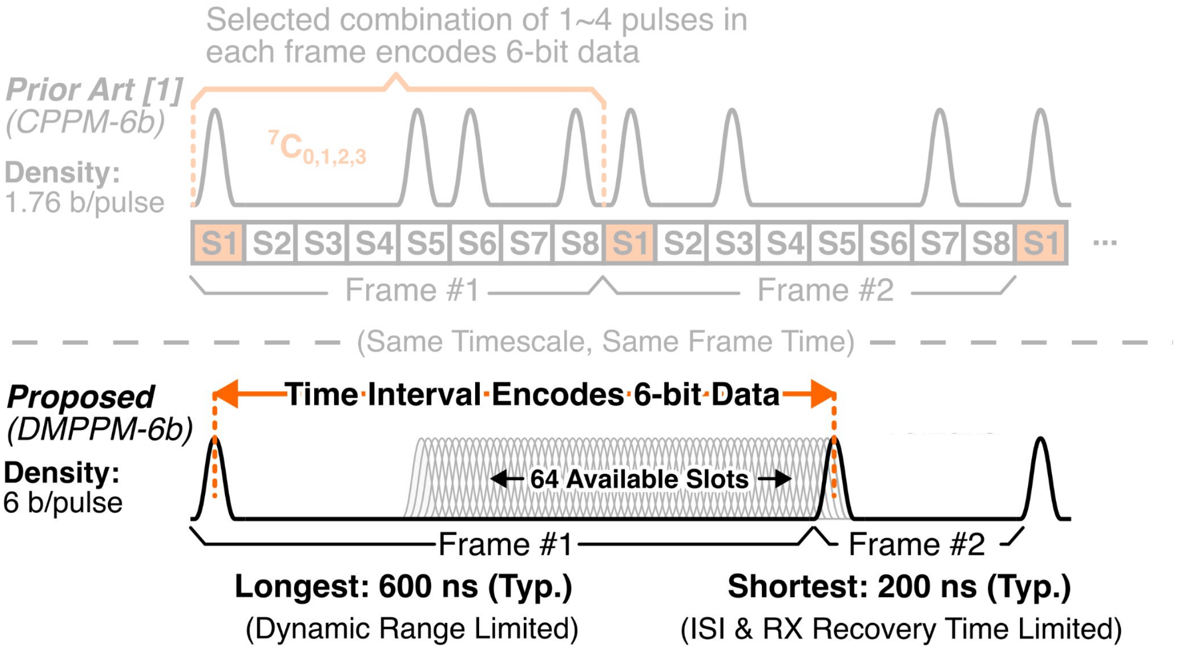
- High Data Rate (~15Mbps)
- Low Power with Even Fewer Switching Activity
- Simple to Design & Calibrate
- FinFET-Friendly Timing Generation
- Lower Clock Speed

High Density Differential-Mode Pulse-Position-Modulation (DM-PPM)



DTC+TDC enables sub-clock period resolution.

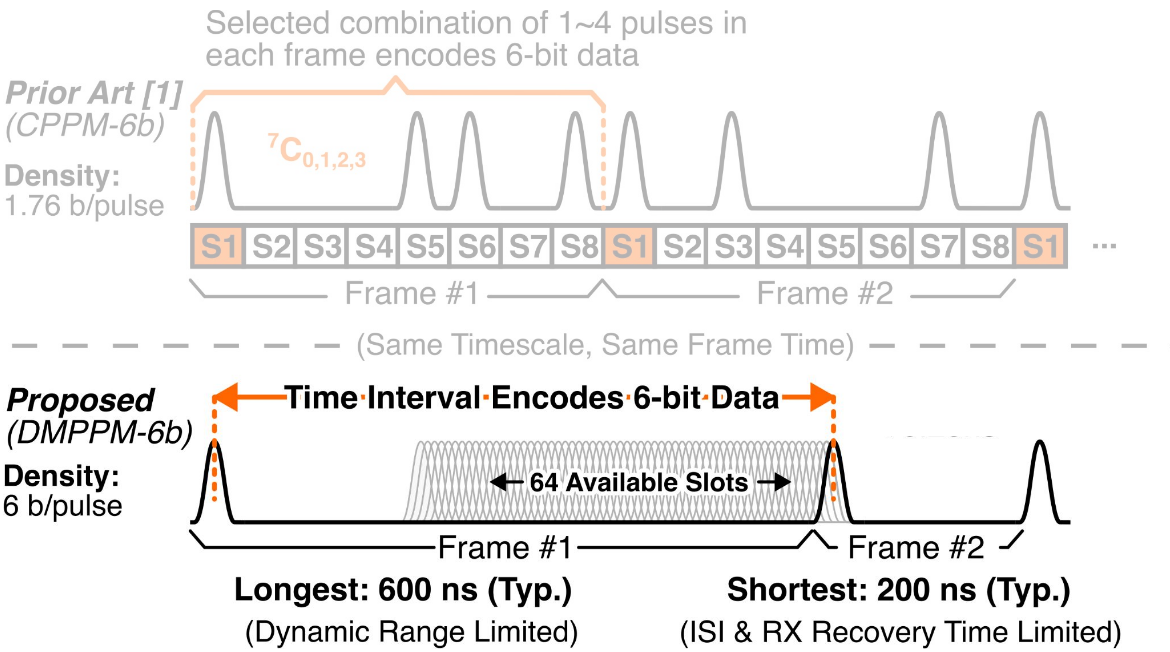
High Density Differential-Mode Pulse-Position-Modulation (DM-PPM)

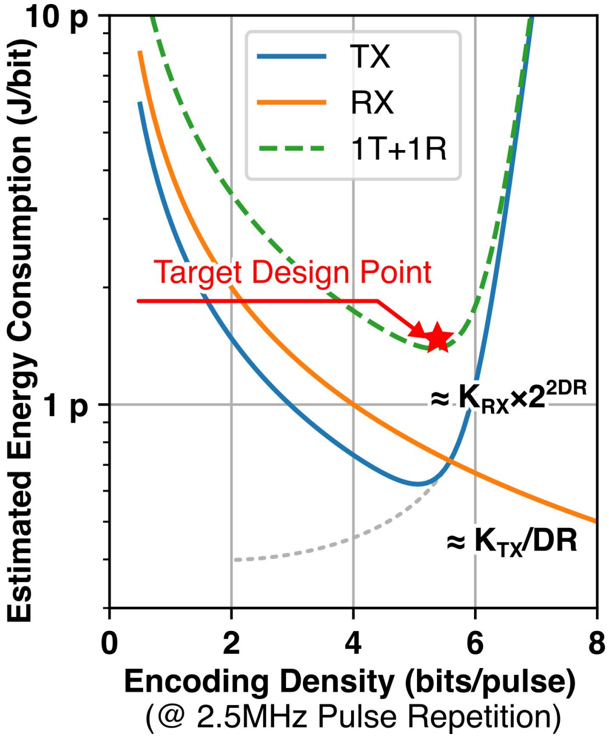


DTC+TDC enables sub-clock period resolution.

How much resolution is appropriate?

High Density Differential-Mode Pulse-Position-Modulation (DM-PPM)





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  - **Resonant Pulse Transmitter**
  - Low Power Receiver
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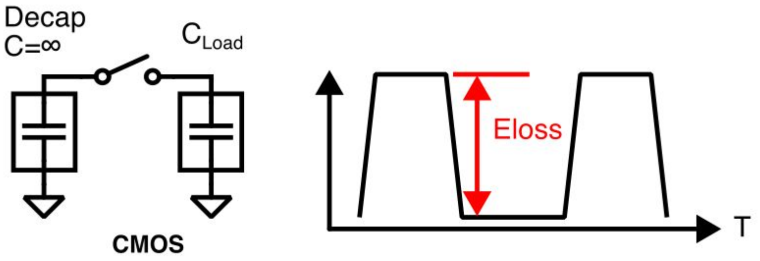
Resonant Pulse Transmitter: Concept



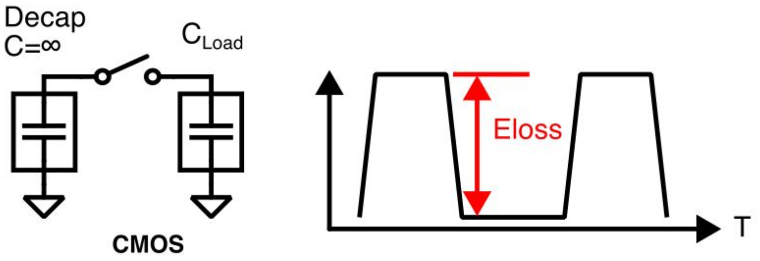
Energy Lost in 1 Cycle:

$E_{loss}=E_{cload}$

Human Skin is a capacitive load
Driving with CMOS will cause 100% capacitive energy loss.

E_{loss} = CV^2 = **25pJ** @ 1.0Vpp per pulse

Resonant Pulse Transmitter: Concept



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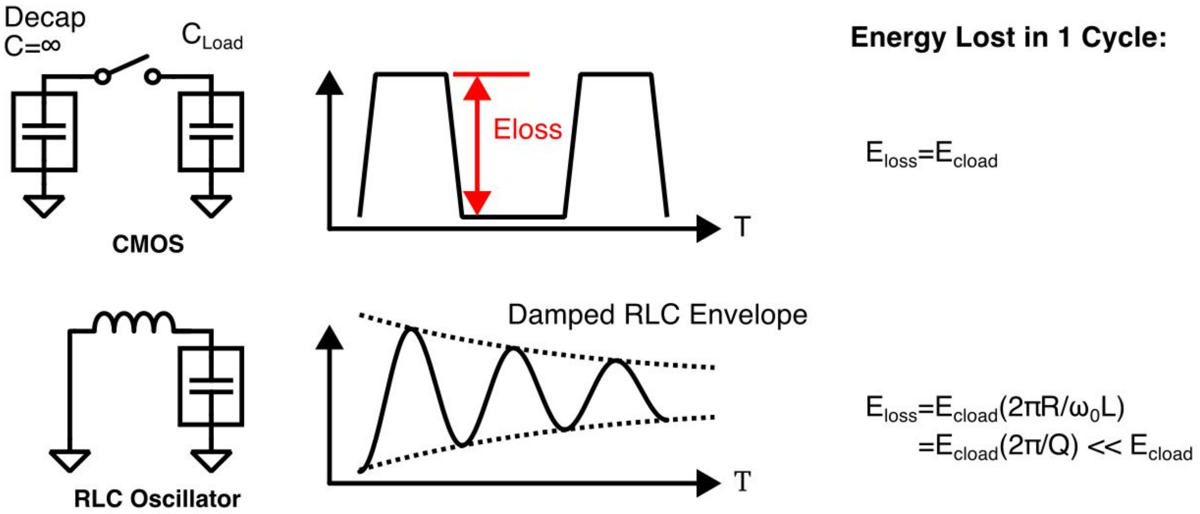
Can we do better?

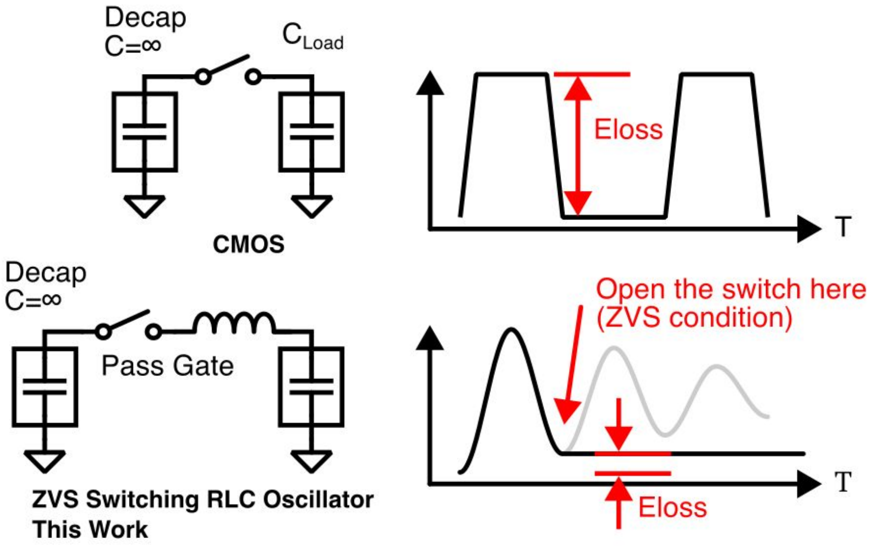
Resonant Pulse Transmitter: Concept



Inductor can create oscillation on a capacitor with lower loss per cycle.

$E_{loss} = E_{cap} \times (2\pi/Q) < 0.13 \times E_{cap}$ = **3.2pJ** @ 1.0Vpp per pulse, Q=50

Resonant Pulse Transmitter: Concept



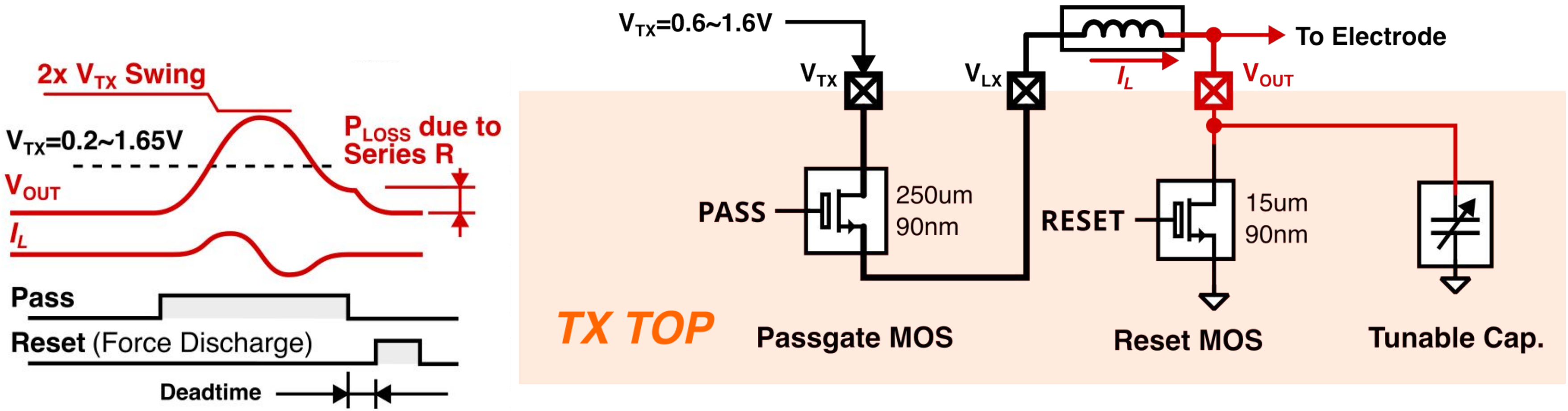
Energy Lost in 1 Cycle:

$E_{loss}=E_{cload}$

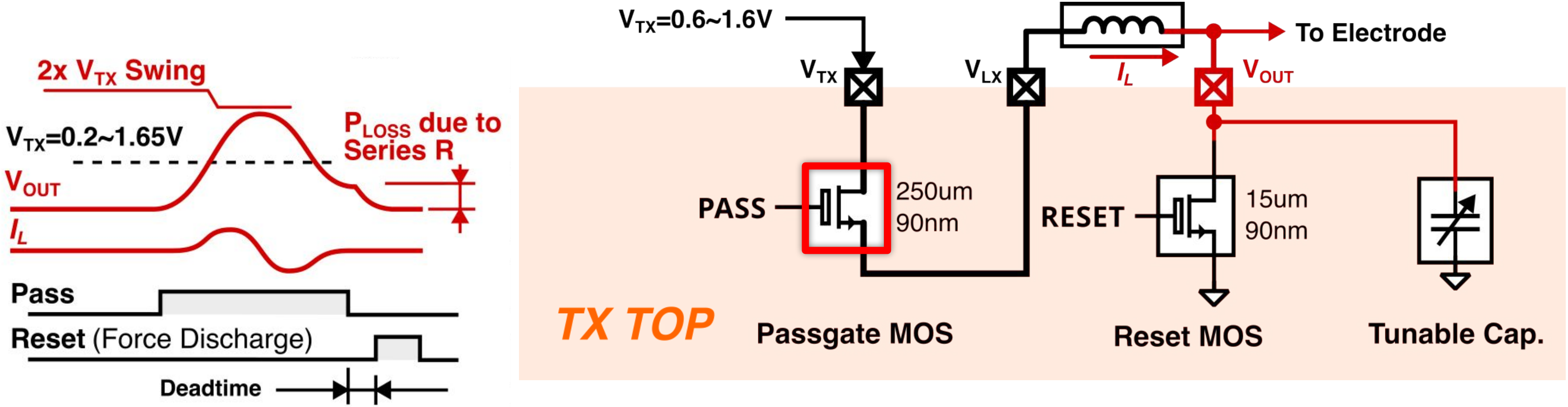
$E_{loss}=E_{cload}(2\pi R/\omega_0 L)$
$=E_{cload}(2\pi/Q) \ll E_{cload}$

The switch can open/close at the peak/valley of the oscillation. without capacitive energy loss (ZVS condition)

Resonant Pulse Transmitter: Simplified Diagram

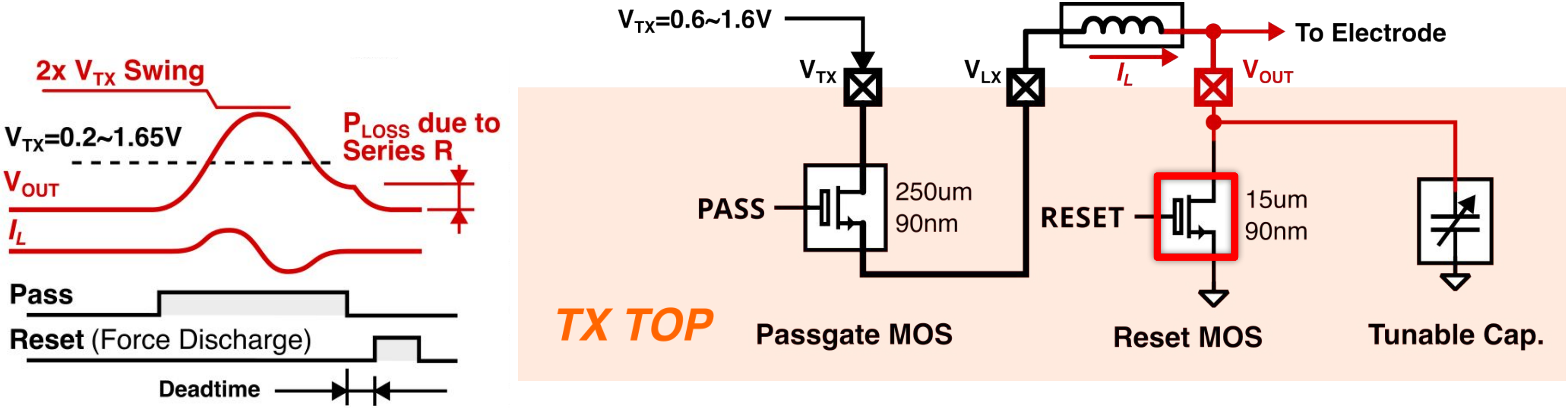


Resonant Pulse Transmitter: Simplified Diagram



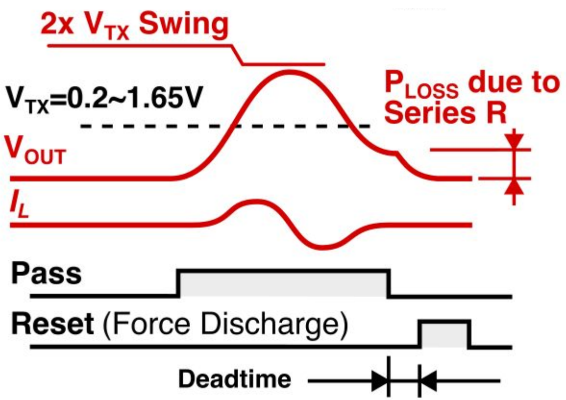
Core switch implemented with a single LVT NMOS 250um width to support up to 5mA peak current.

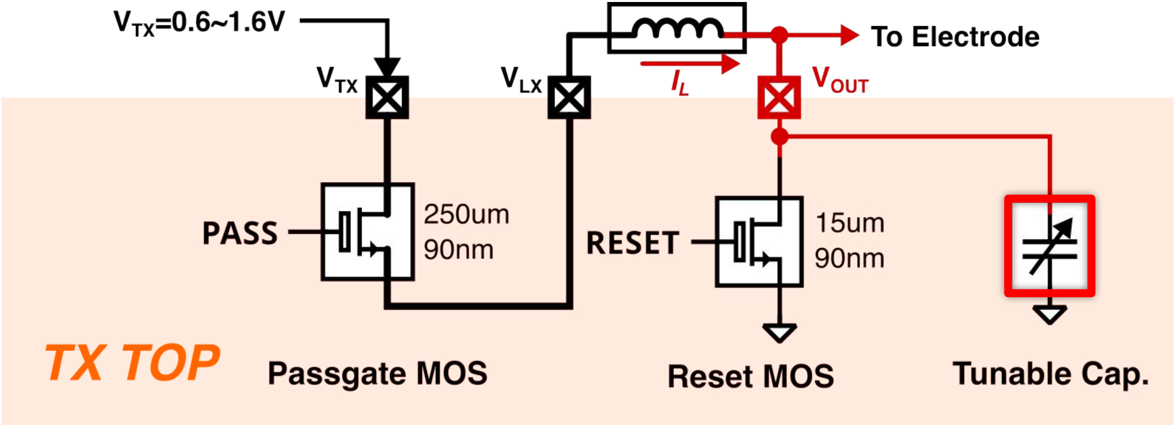
Resonant Pulse Transmitter: Simplified Diagram



Discharge switch discharges the residue voltage, forces the output to 0V when idle.

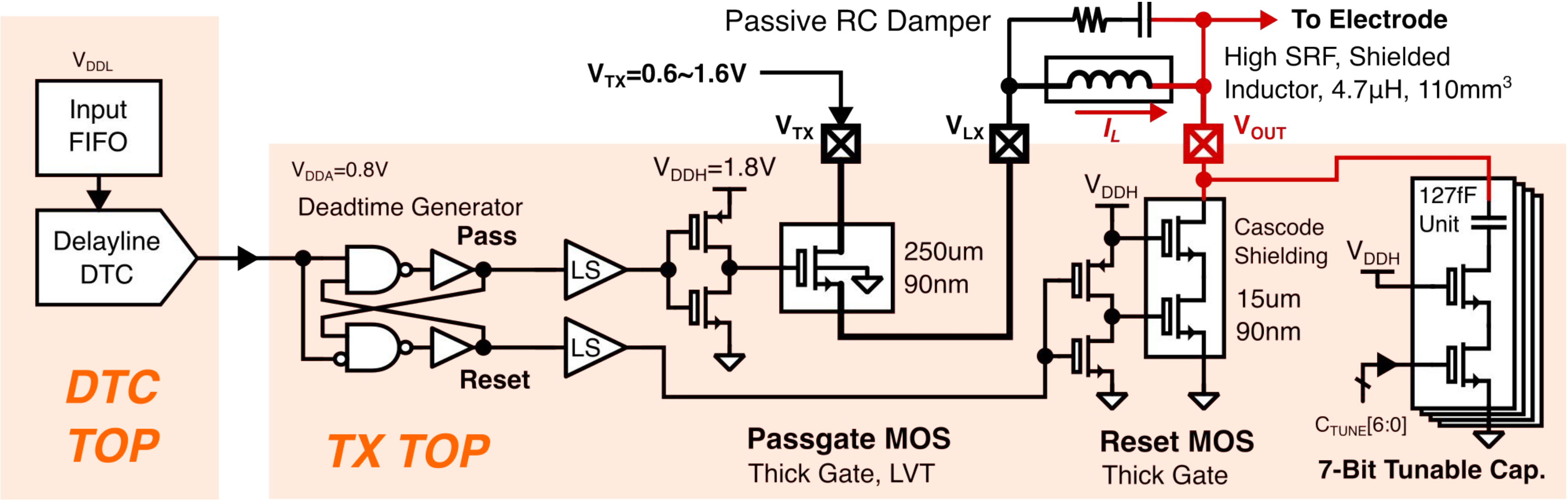
Resonant Pulse Transmitter: Simplified Diagram





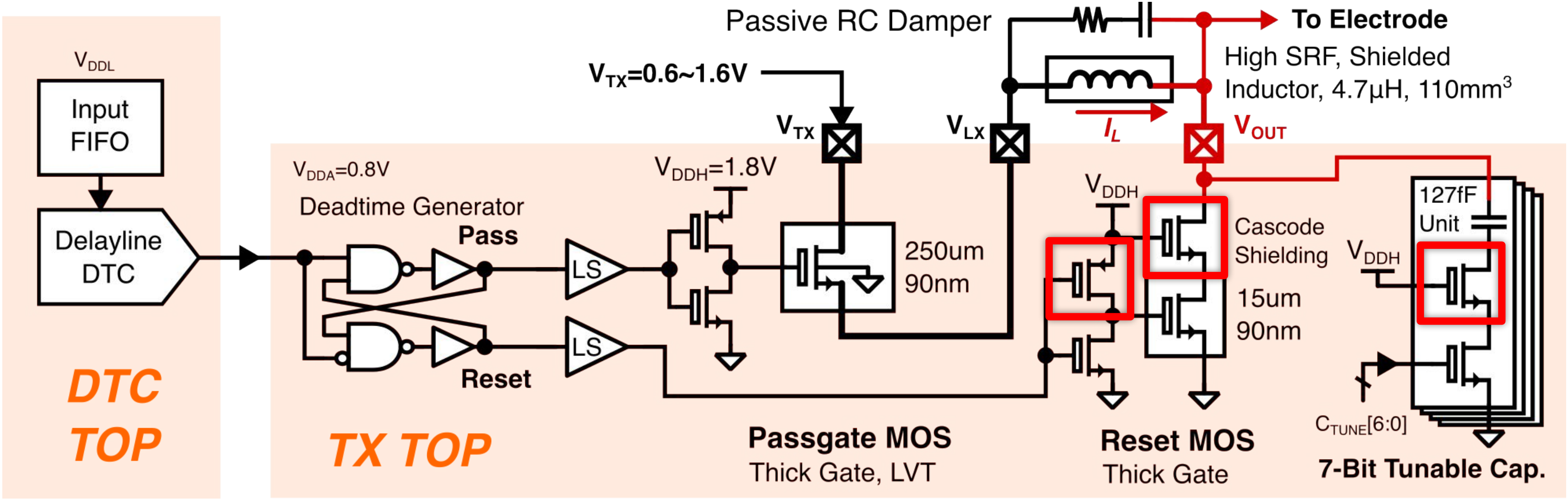
16pF tunable capacitor for resonant frequency trimming

Resonant Pulse Transmitter: Complete Diagram



Complete Circuit Diagram with
DTC, Dead-time Generator, and Level-Shifters (LS)

Resonant Pulse Transmitter: Complete Diagram



Circuit near V_{OUT} has shielding
to support up to **2xVDDIO = 3.6V** output amplitude

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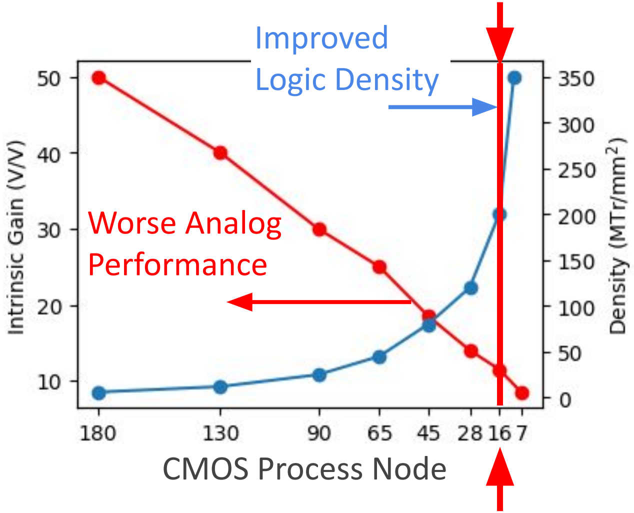
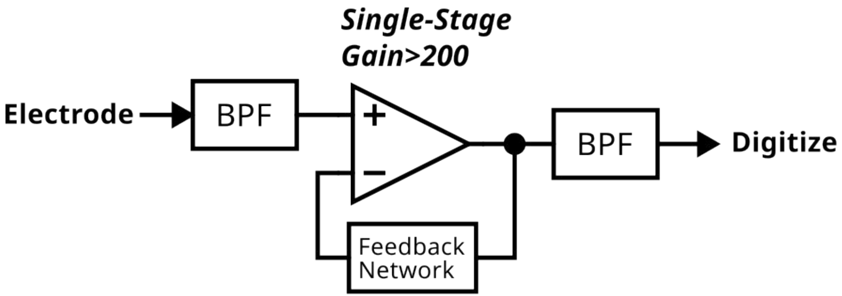
Low Power Receiver: FinFET LNA Design

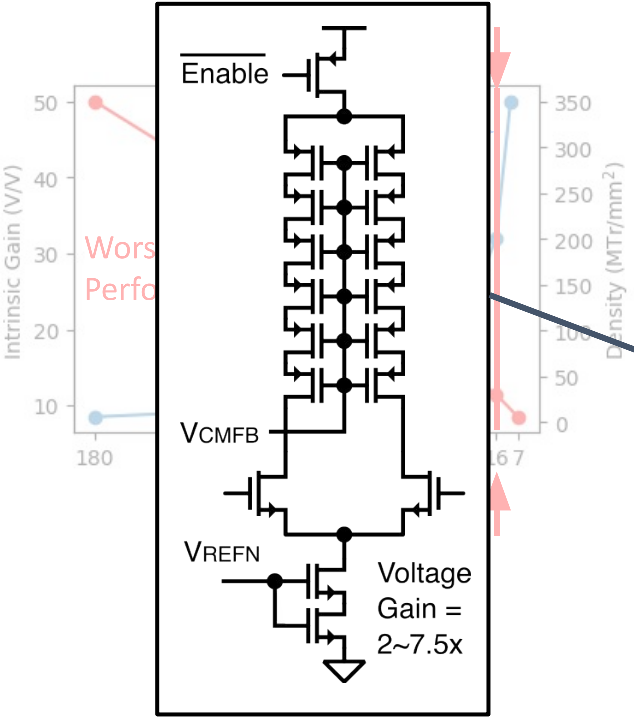




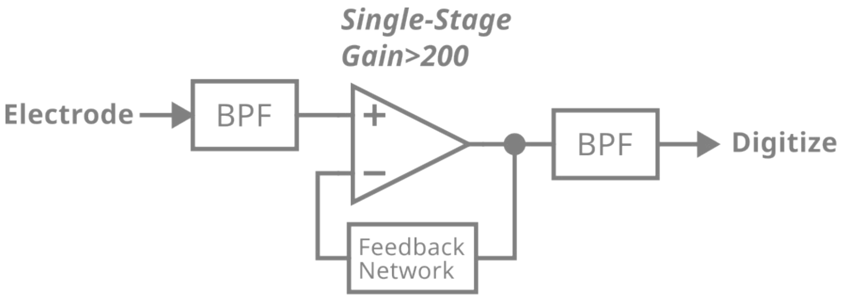
Abstracted LNA Design from Prior Arts. [1,6~9,10]

Intrinsic gain in 16nm is only 10V/V !
Hard to achieve high gain with 1 stage.

Low Power Receiver: FinFET LNA Design



Basic 5-T OTA Impl. in FinFET



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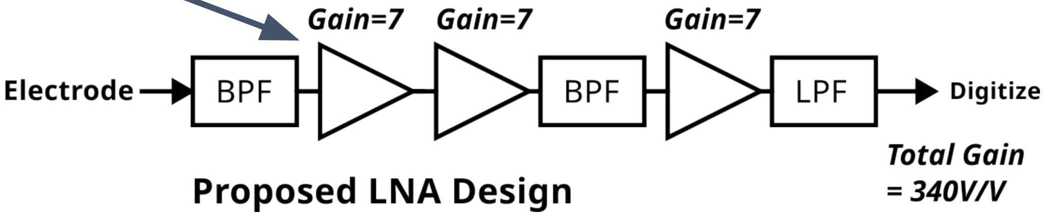
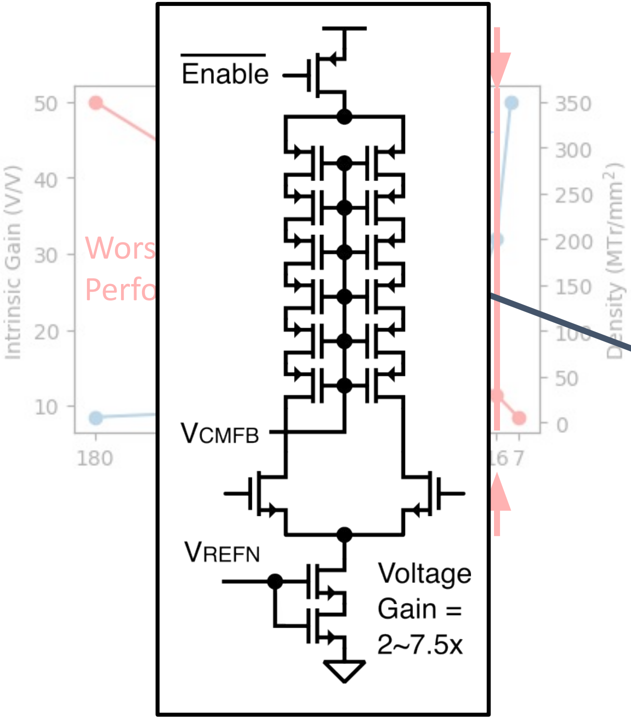


Proposed LNA Design

Each stage only need to provide 7V/V gain

Latency is negligible from a system perspective.

Low Power Receiver: FinFET LNA Design



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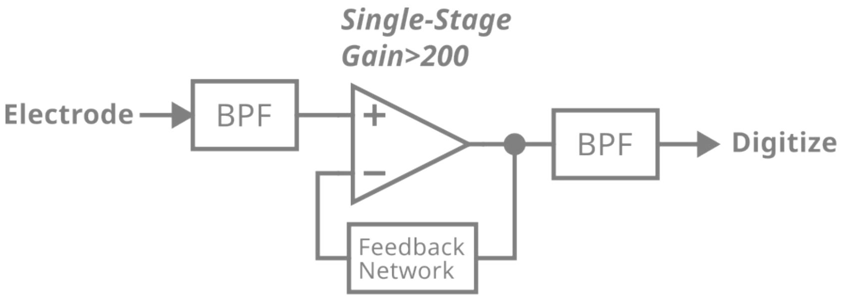

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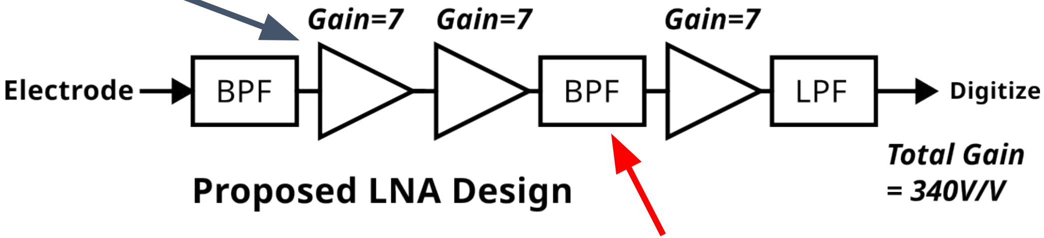
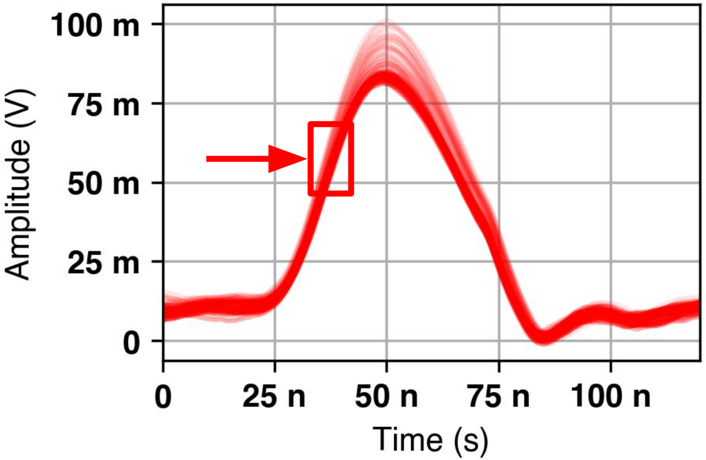


Proposed LNA Design

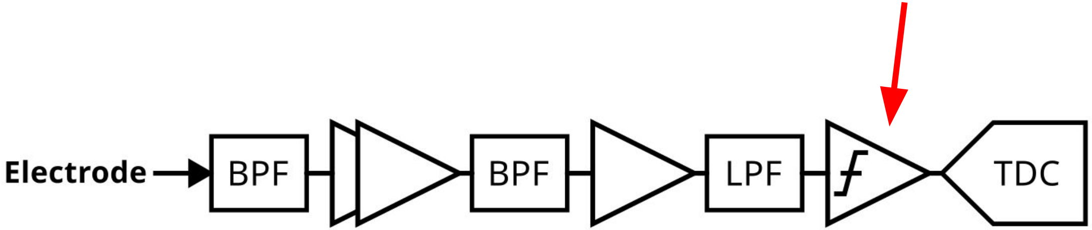
BPF/HPF Removes DC Offset

Offset trimming not required.

Low Power Receiver: Amplitude Variation Rejection



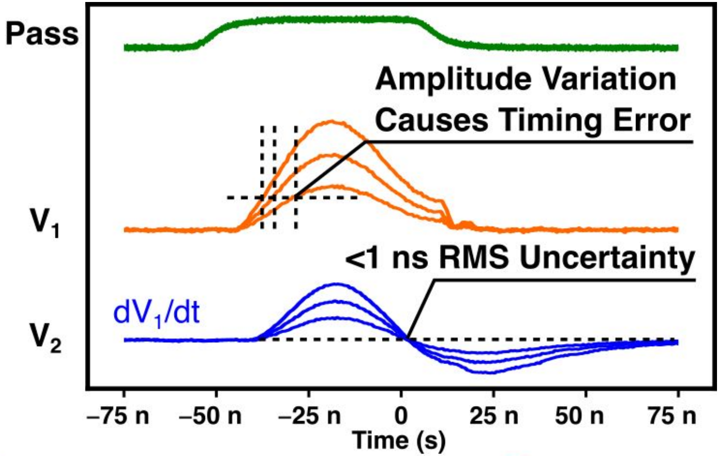
Amplitude Variation
to Timing Error Conversion



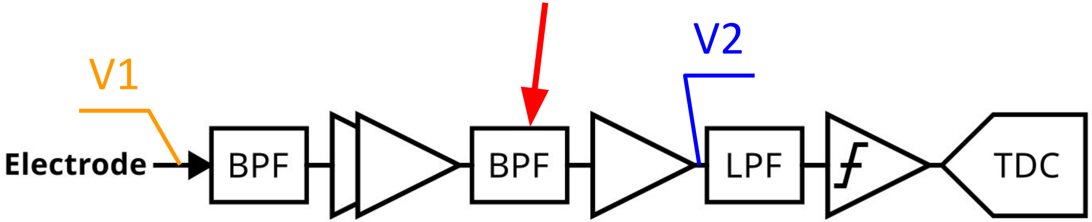
Proposed RX Front-End Design

Amplitude variation causes
>4 ns timing error

Low Power Receiver: Amplitude Variation Rejection



Reusing Tuned-BPF as a differentiator (dV/dt) [4]



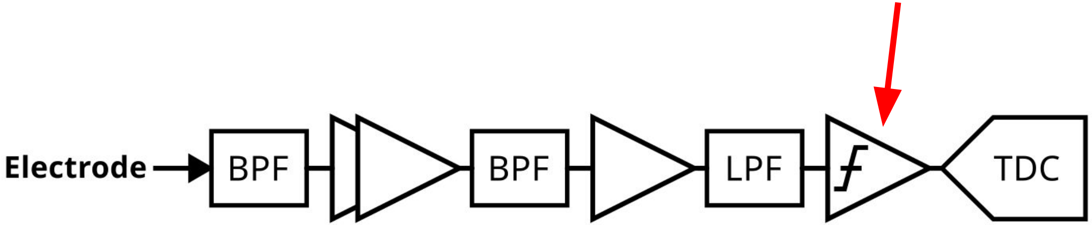
Proposed RX Front-End Design

✅ Reduces timing error in practical setups to enable 6b/pulse

❌ -3dB SNR Penalty

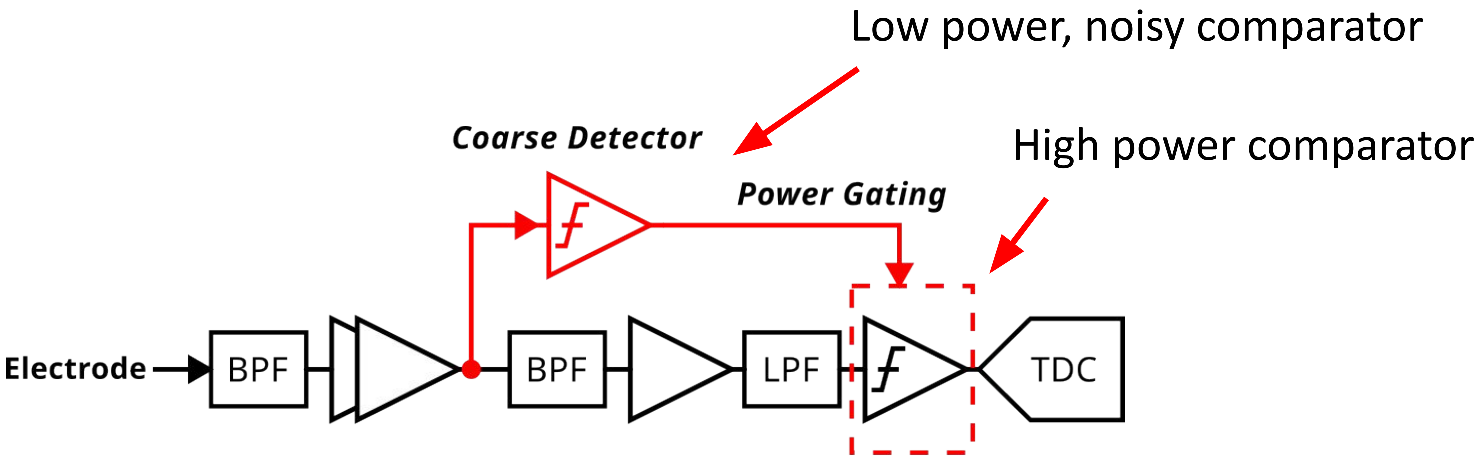
Low Power Receiver: Power Gating

Very high power (20uW) compared to the other stages



Proposed RX Front-End Design

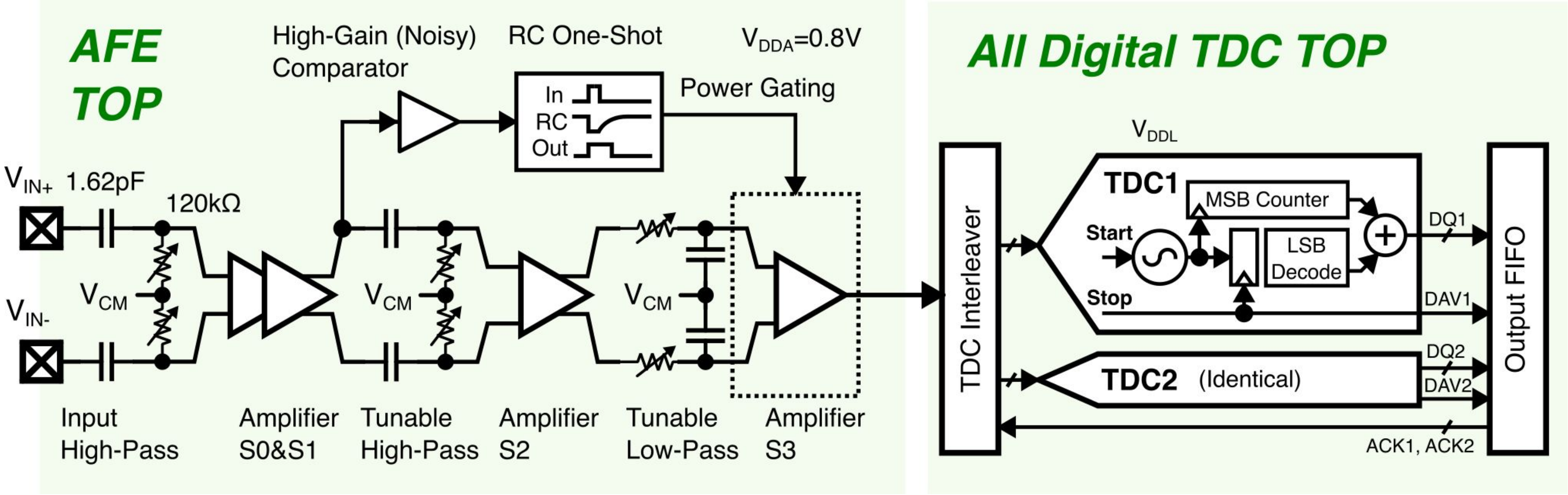
Low Power Receiver: Power Gating



Proposed RX Front-End Design

Proposed Solution: Use delay to our advantage.
Rising edge is non-critical. Use it to power gate the falling edge detector.

Low Power Receiver: Complete Diagram



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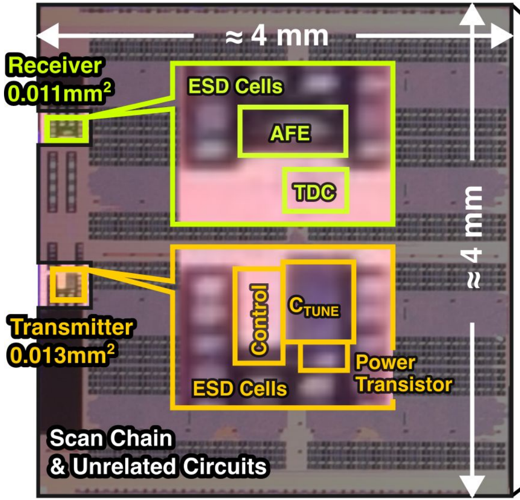
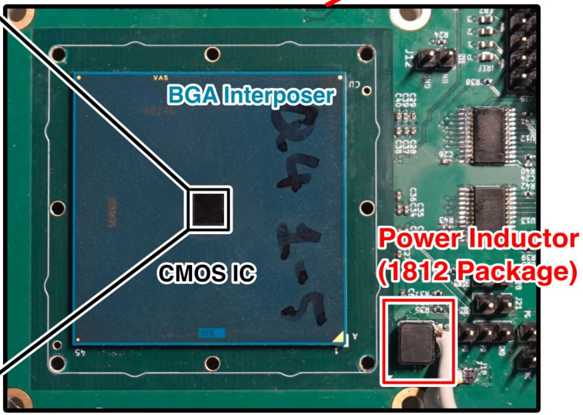
Chip & Test Board Photograph

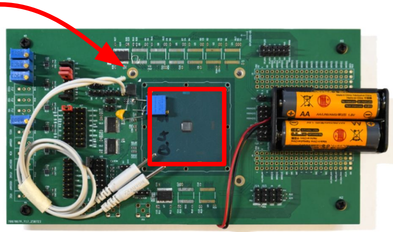


Process Node: 16nm
Package: Flip-Chip BGA

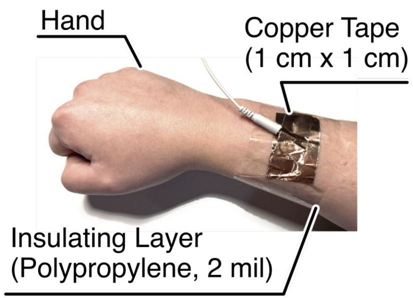
Chip Micrograph & Assembly



PCB Photograph

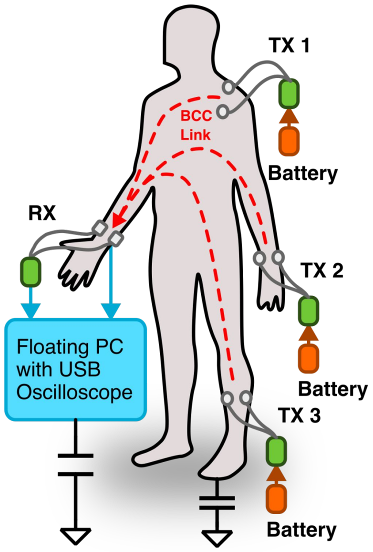


Battery Powered TX Board

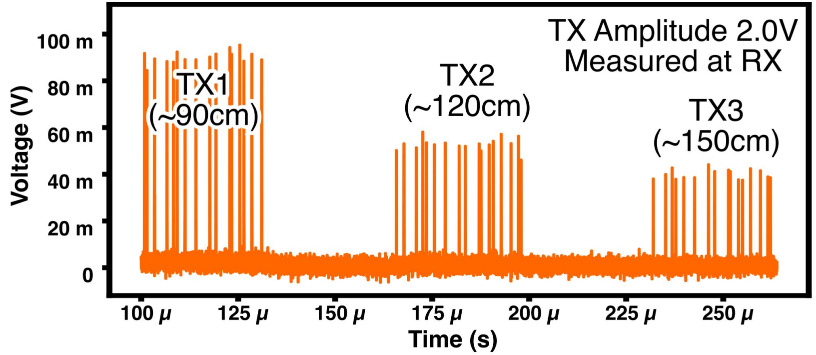


Electrode Structure

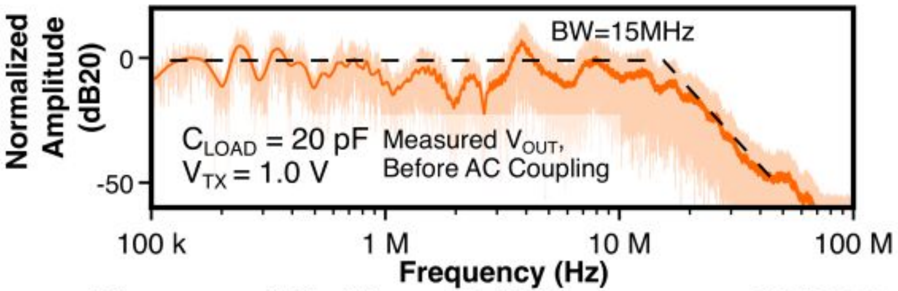
Measurements



Multi-Node TX Setup

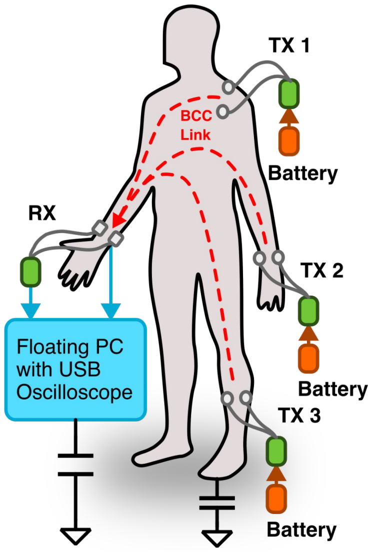


Measured TDMA Waveform of PRBS Data



Measured Unfiltered TX Spectrum of PRBS

Measurements



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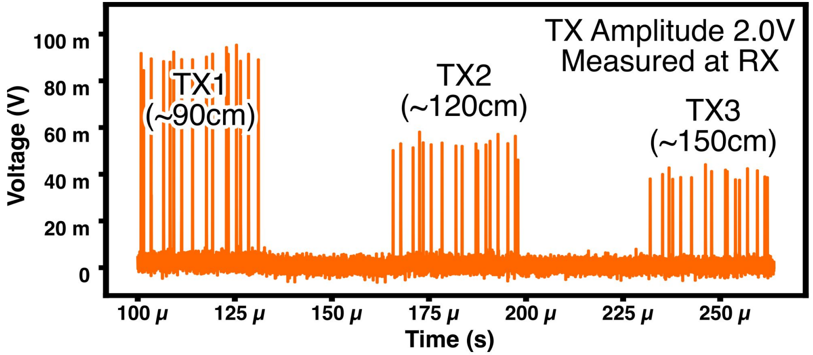

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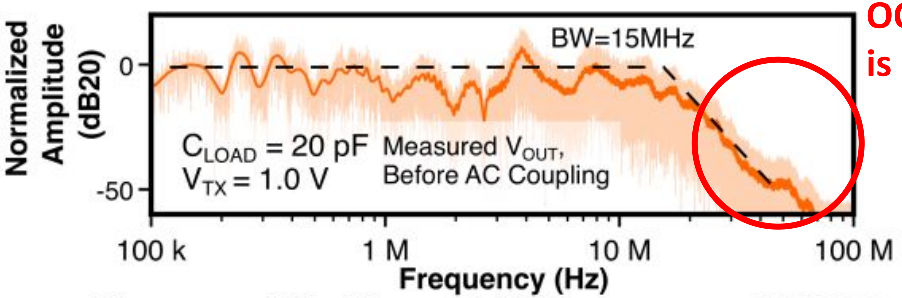
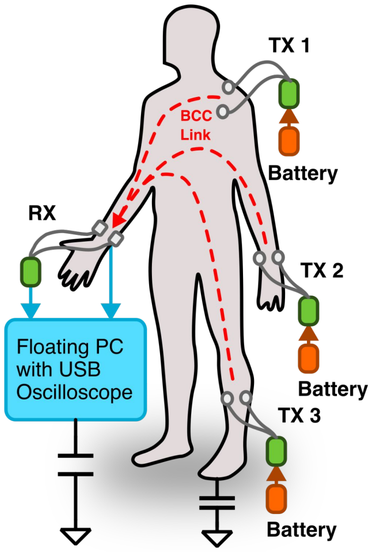


OOB leakage is attenuated

Measured Unfiltered TX Spectrum of PRBS

Measurements



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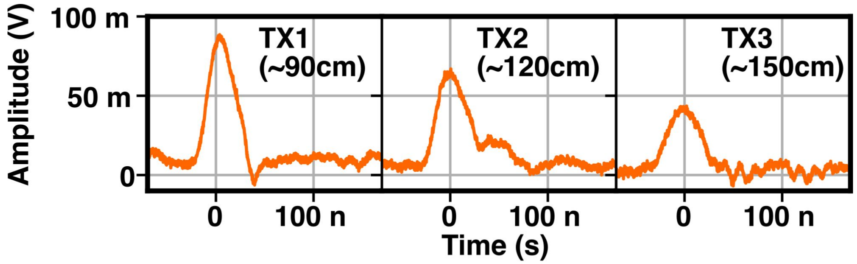
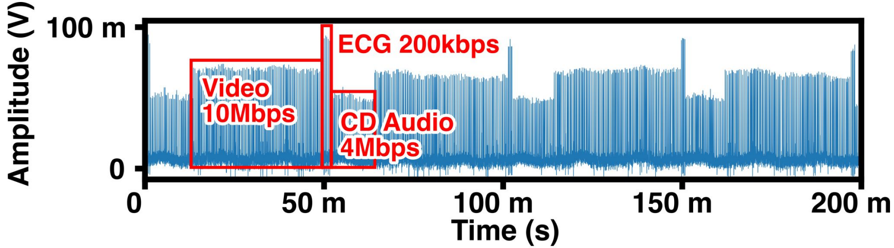
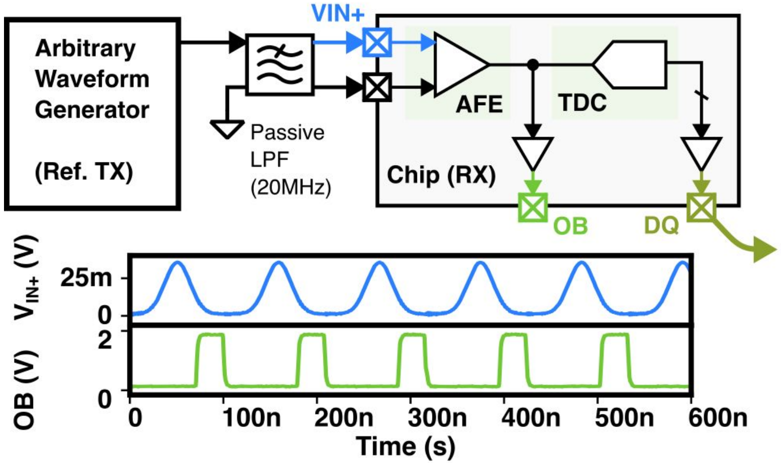


Measured Waveform at RX

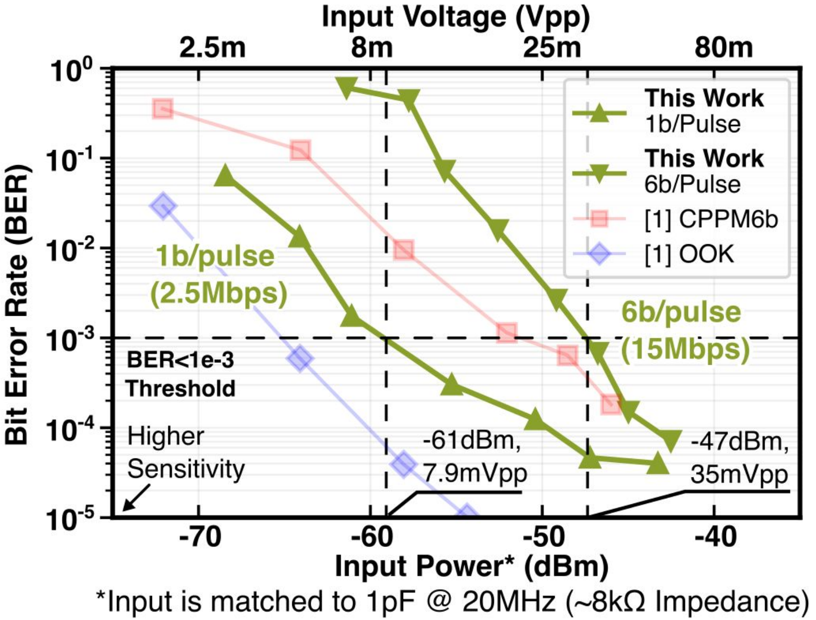


Measured Multi-Node Transaction Demo

Measurements

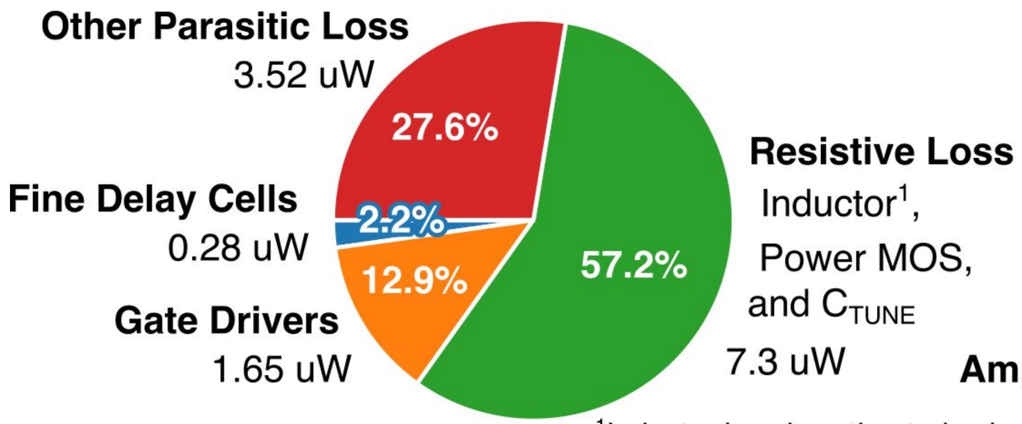


RX Performance Measurement Setup

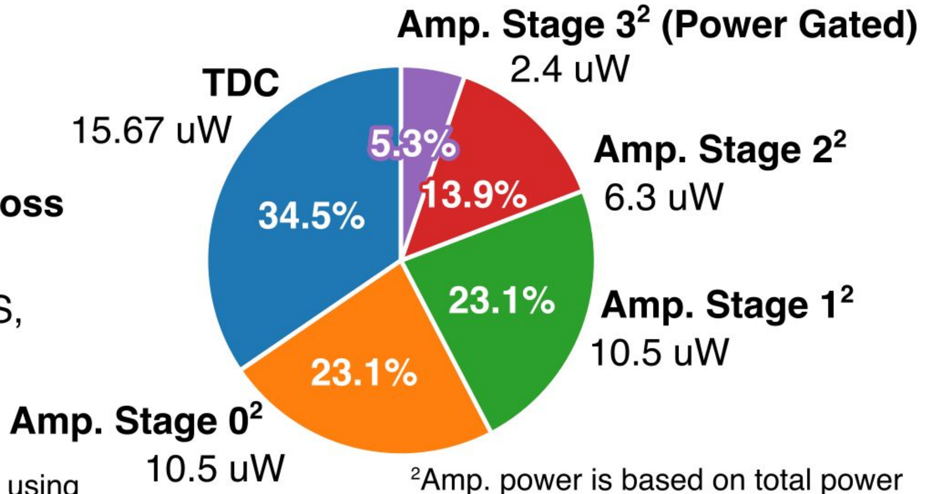


Measured RX Sensitivity vs. Input Power

Conclusion: Power Breakdown



[1]Inductor loss is estimated using vendor's electrical model



[2]Amp. power is based on total power measured × simulated percentage

Conclusion

Paper	This Work	B.Chatterjee, ISSCC'22 [1]	N. Modak, CICC'21 [6]	S.Maity, JSSC'21 [7]	J. Park, ISSCC'19 [8]	S.Maity, JSSC'19 [9]
Technique	Inductor Resonance	Adiabatic Switching	Inductor Resonance	CMOS Push-Pull	Push-Pull, Magnetically Coupled	CMOS Push-Pull
Modulation	DMPPM6b	CPPM (3~6b)	OOK	OOK	OOK	NRZ
Demod. Method	TDC + DTC	CDR	CDR	CDR	Envelope Detect	CDR
Carrier Freq.	15 MHz	20 MHz	0.5~2 MHz	0.05~1 MHz	40 MHz	-
Data Rate (Mbps)	2.5~15	7.5~15	0.001~0.02	0.001~0.02	5	30
VDD (V)	0.8	0.75	0.5	0.5	0.6	1
Maximum TX Amplitude w/o Stress (V)	3.3	0.7	10	0.5	-	-
Best TX Efficiency (pJ/b)	0.85 (6 b/pulse)	4.2 (NRZ CPPM-6b)	169	277.9	11.2	34.9
Best RX Efficiency (pJ/b)	3.2 (6 b/pulse)	4.0 (NRZ CPPM-6b)	3.6	140	4.8	3.27 (w/o Clock)
TX Power (uW)	12.75	63	1.5	2.47	35.8	2600
RX Power (uW)	48	60	72	1.4	24	98
Area (mm2)	RX: 0.011 TX: 0.013	0.259	0.13	0.3375	0.12	-
Process Node	16nm	65nm	65nm	65nm	65nm	65nm
Sensitivity (dBm)	-47 (6 b/p) -61 (1 b/p)	-65 (OOK) -52 (CPPM)	-60	-64	-56	-64
BER Target	1E-3	1E-3	1E-5	1E-3	1E-3	1E-3

Conclusion

Supports High Data Rate Applications

Paper	This Work	B.Chatterjee, ISSCC'22 [1]	N. Modak, CICC'21 [6]	S.Maity, JSSC'21 [7]	J. Park, ISSCC'19 [8]	S.Maity, JSSC'19 [9]
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BER Target	1E-3	1E-3	1E-5	1E-3	1E-3	1E-3

Conclusion

High TX Amplitude (2x IO transistor breakdown voltage)

Paper	This Work	B.Chatterjee, ISSCC'22 [1]	N. Modak, CICC'21 [6]	S.Maity, JSSC'21 [7]	J. Park, ISSCC'19 [8]	S.Maity, JSSC'19 [9]
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Modulation	DMPPM6b	CPPM (3~6b)	OOK	OOK	OOK	NRZ
Demod. Method	TDC + DTC	CDR	CDR	CDR	Envelope Detect	CDR
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BER Target	1E-3	1E-3	1E-5	1E-3	1E-3	1E-3

Conclusion

High Power Efficiency: 2.2pJ/b assuming 50% TX, 50% RX

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Modulation	DMPPM6b	CPPM (3~6b)	OOK	OOK	OOK	NRZ
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BER Target	1E-3	1E-3	1E-5	1E-3	1E-3	1E-3

Conclusion

Small On-Chip Area

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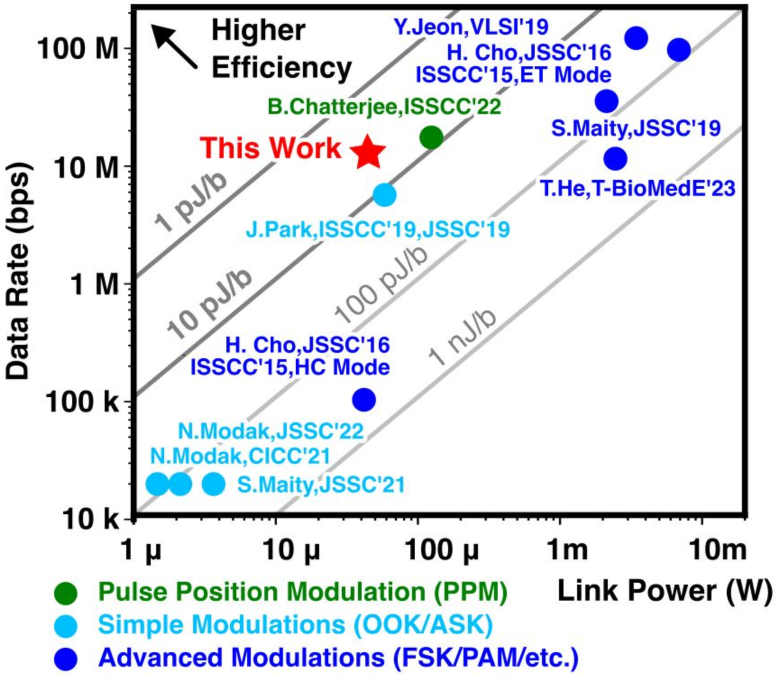
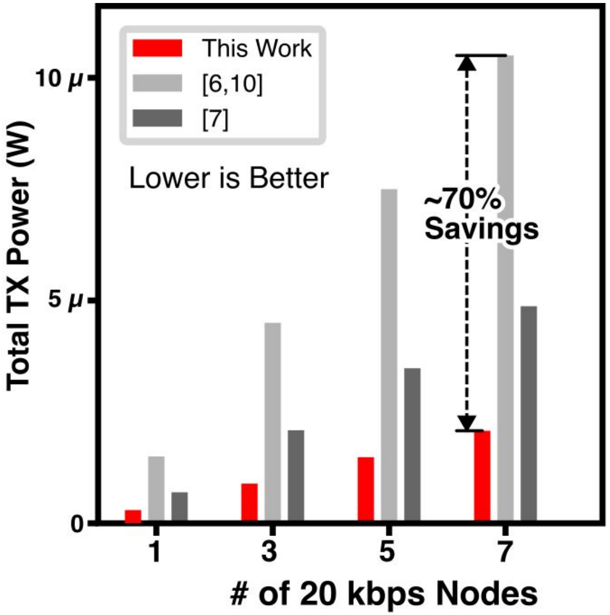
BER Target	1E-3	1E-3	1E-5	1E-3	1E-3	1E-3

Conclusion



Energy Efficiency Plot of Recent HBC Transceivers



*Assuming TDMA for this work, FDMA for others; Leakage is included

Power Estimation of Low-Speed Multi-Node Applications

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